20070705

FIG.1

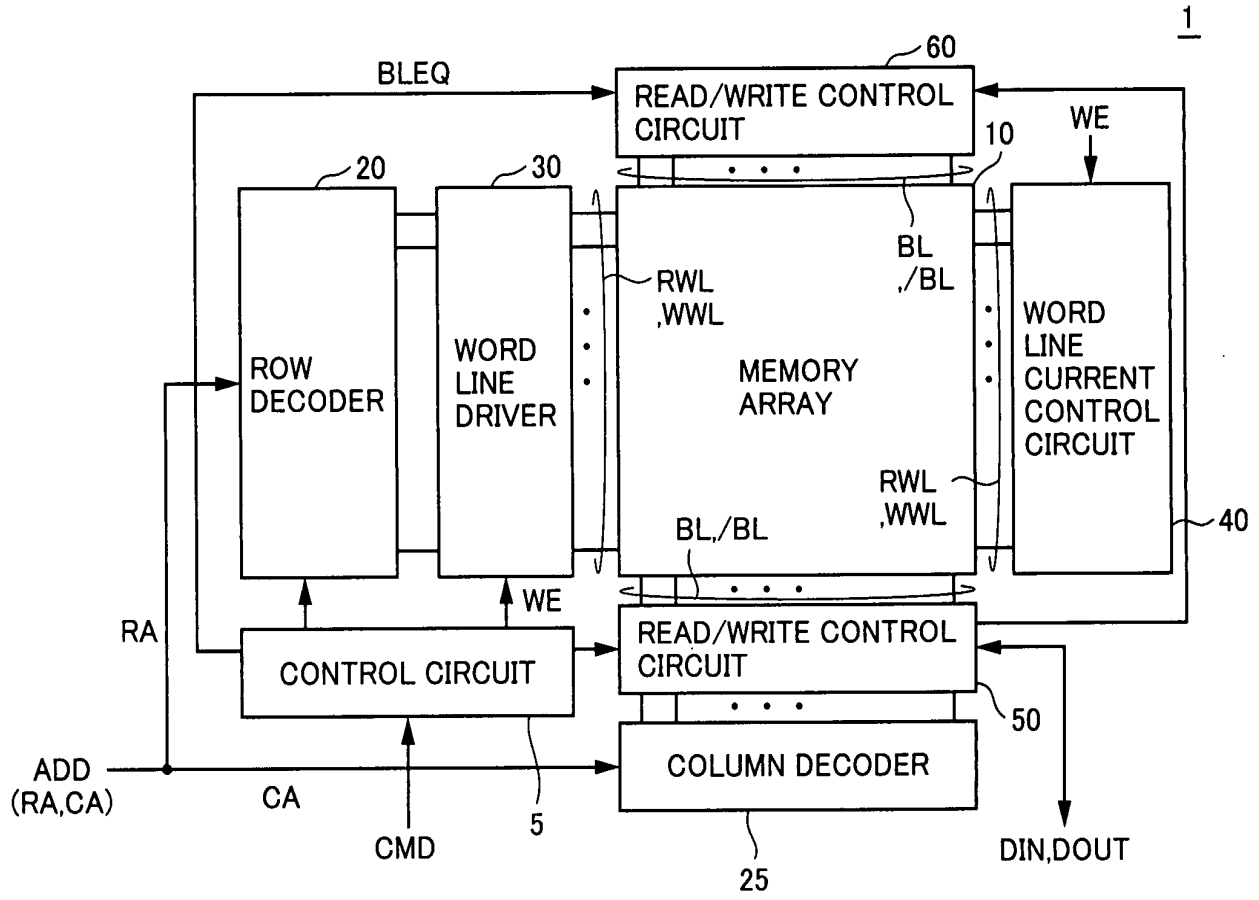

FIG.2

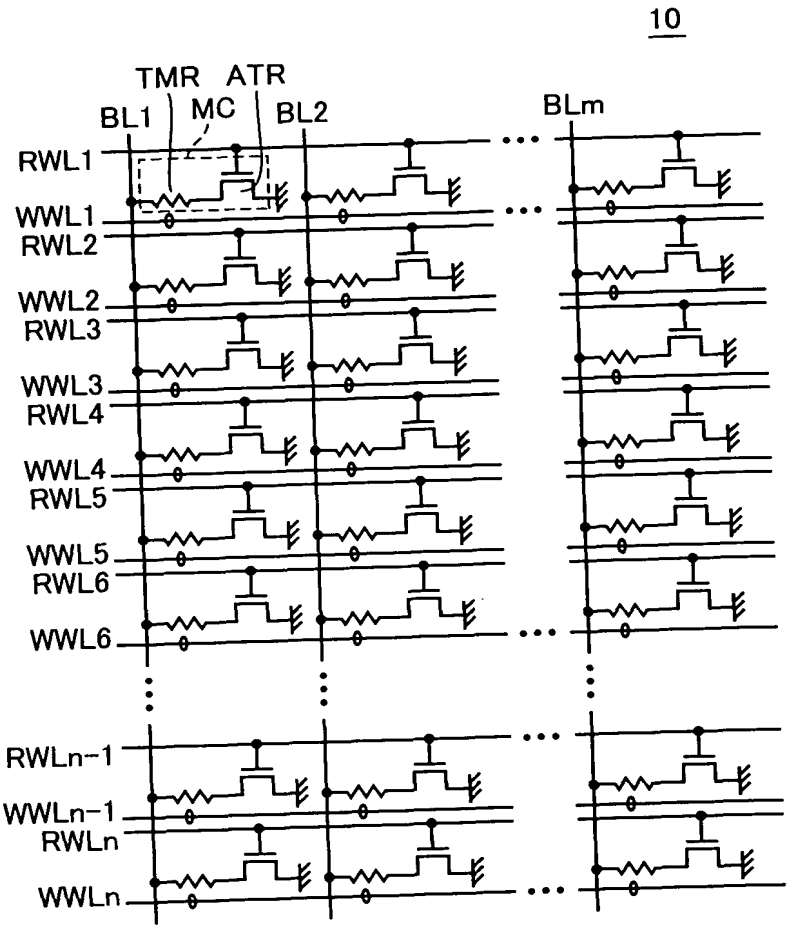
10
TMR
ATR
MC
BL1
BL2
BLm
RWL1
WWL1
RWL2
WWL2
RWL3
WWL3
RWL4
WWL4
RWL5
WWL5
RWL6
WWL6
RWLn-1
WWLn-1
RWLn
WWLn

FIG.3

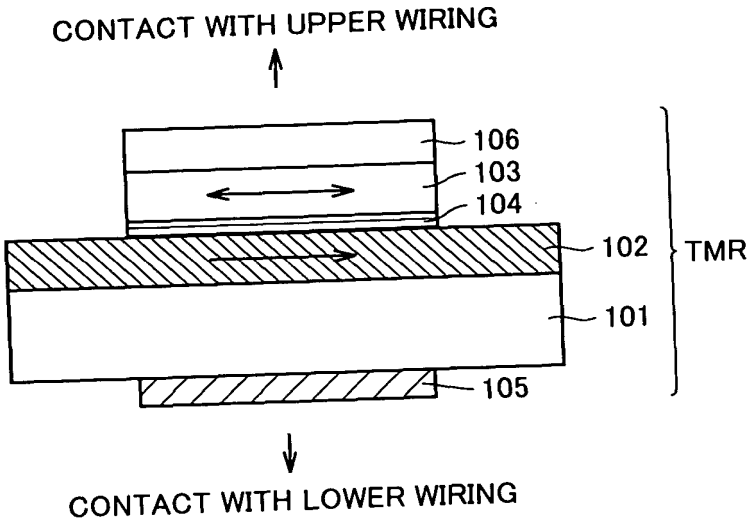

FIG.4

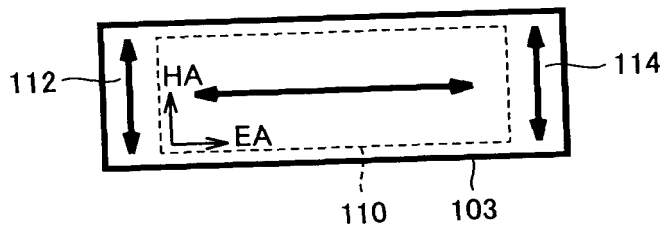

FIG.5

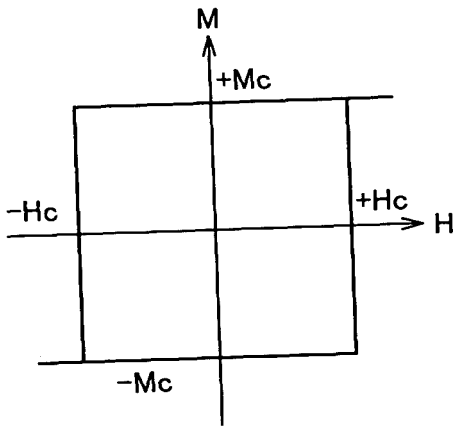

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FIG.6

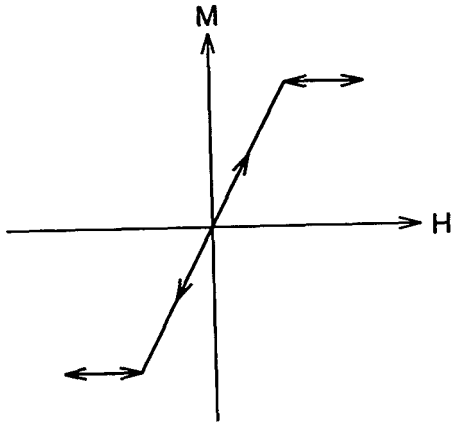

FIG.7

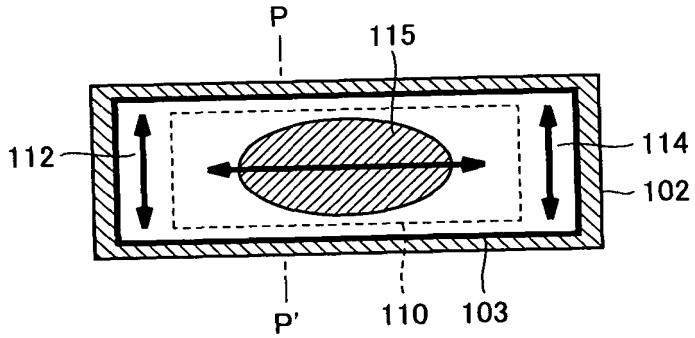

FIG.8

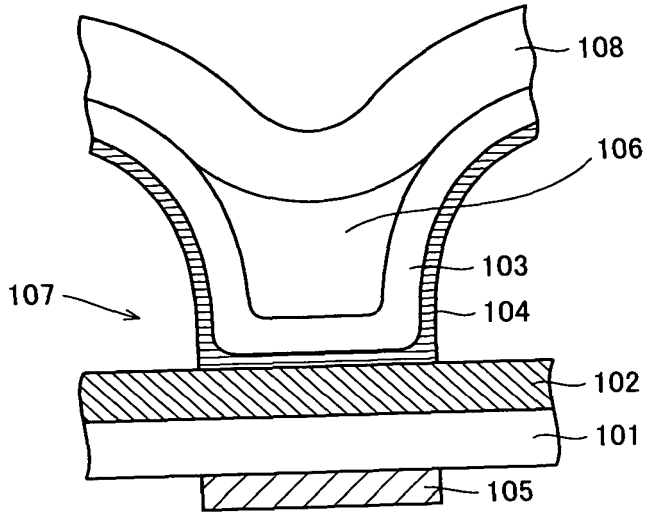

FIG.9

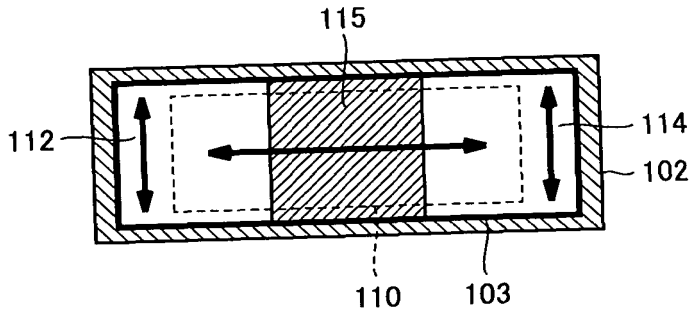

FIG.10

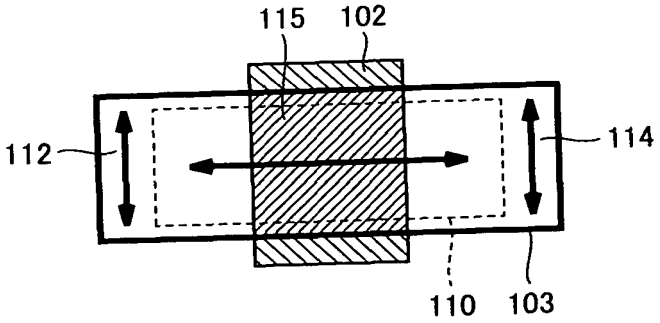

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FIG.11

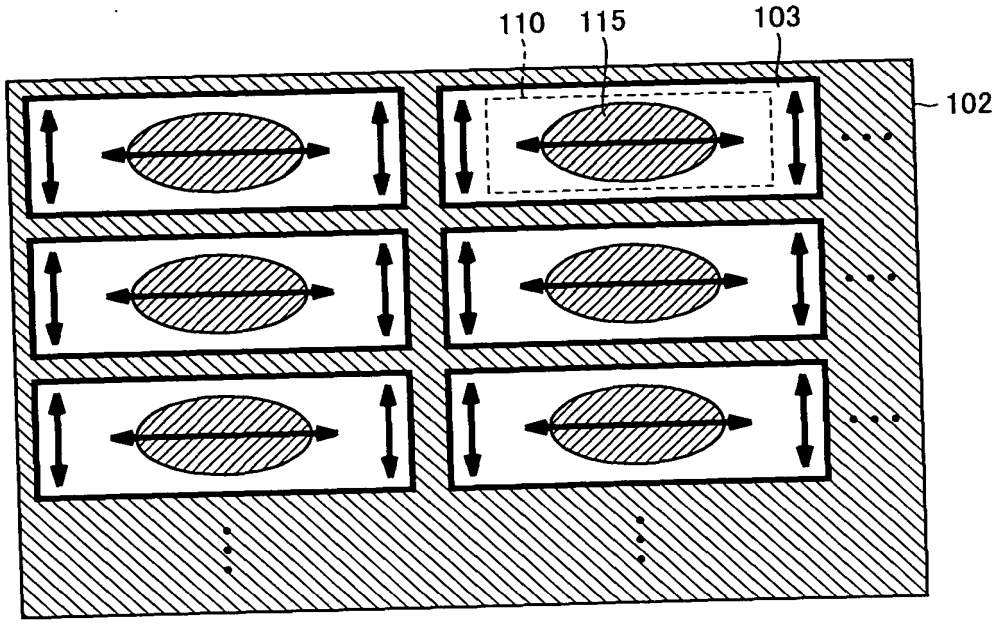

FIG.12

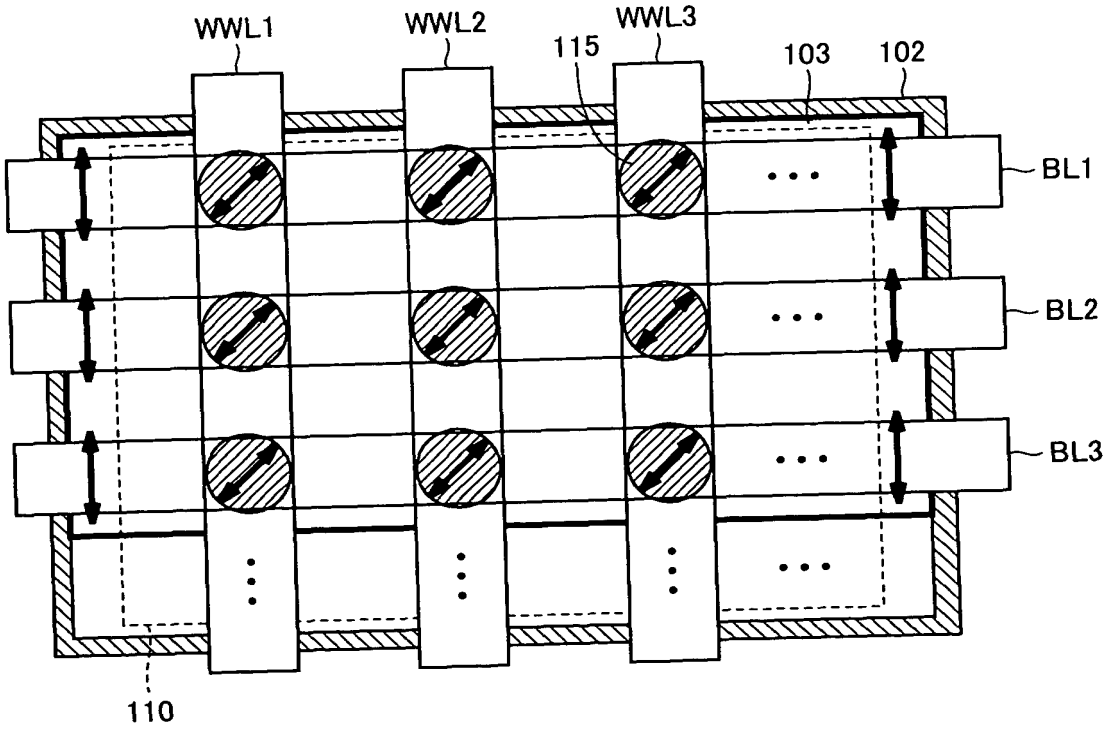

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FIG.13

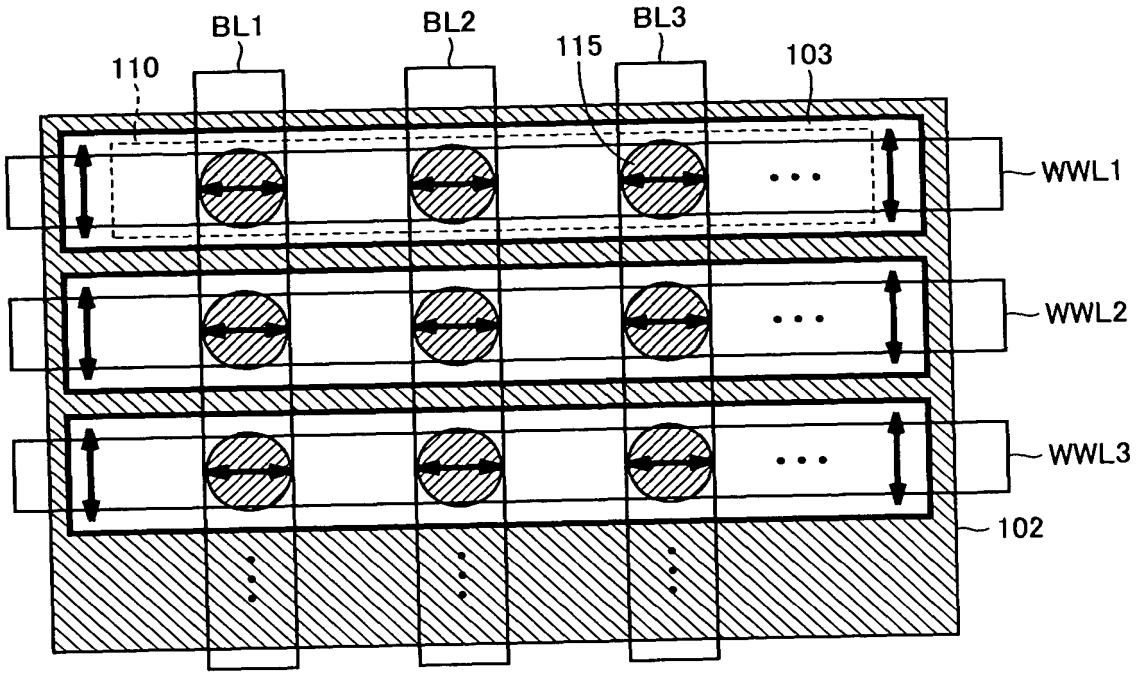

FIG.14

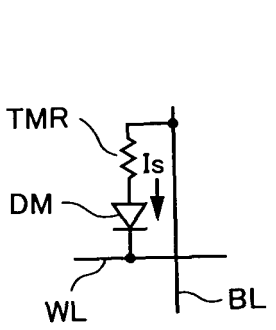

FIG.15

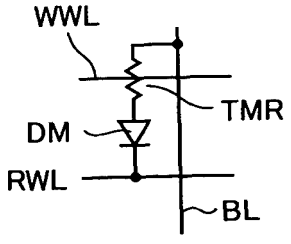

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FIG.16

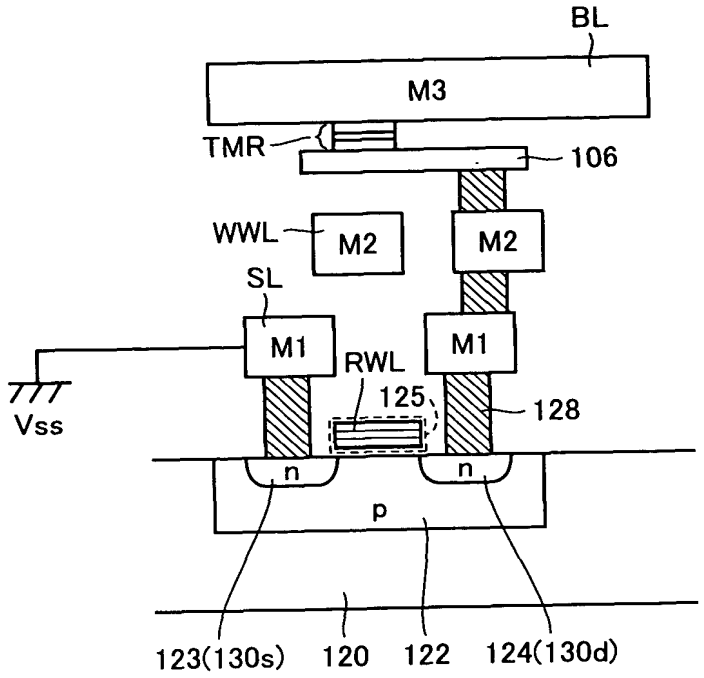
BL
M3
TMR
106
WWL
M2
M2
SL
M1
RWL
M1
125
128
Vss
n
n
p
123(130s)
120
122
124(130d)

FIG.17

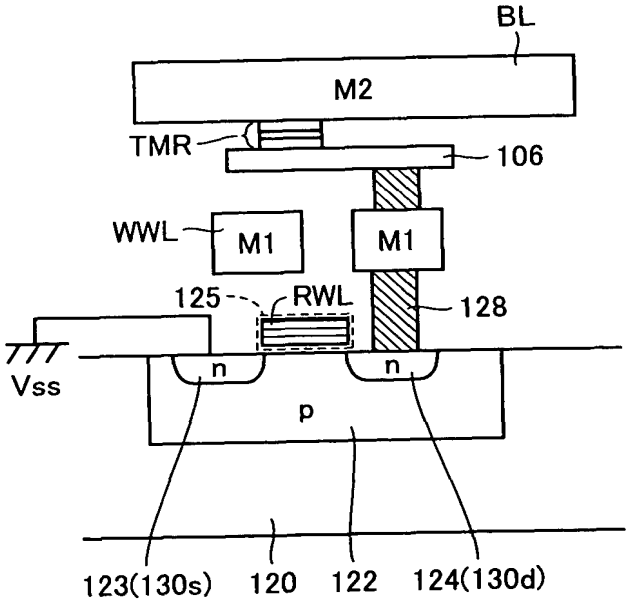
BL
M2
TMR
106
WWL
M1
M1
125
RWL
128
Vss
n
n
p
123(130s)
120
122
124(130d)

FIG.18

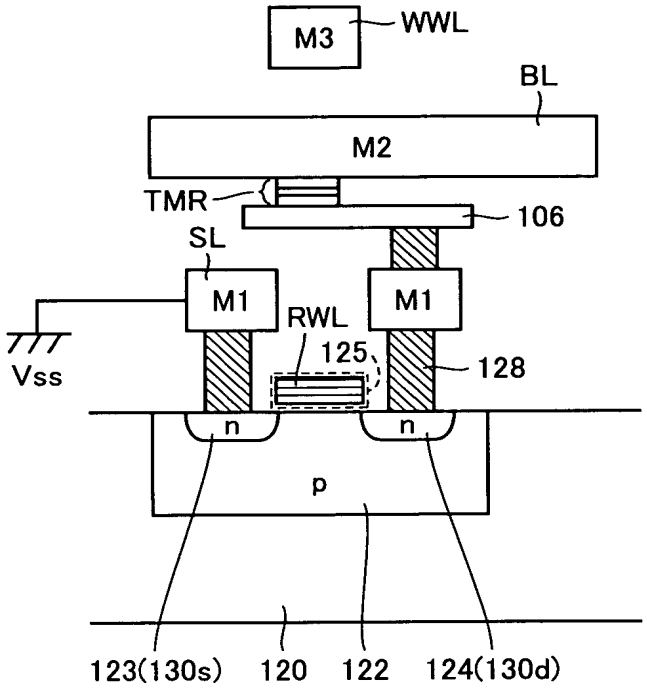
M3
WWL
BL
M2
TMR
106
SL
M1
M1
RWL
125
128
Vss
n
n
p
123(130s)
120
122
124(130d)

FIG.19

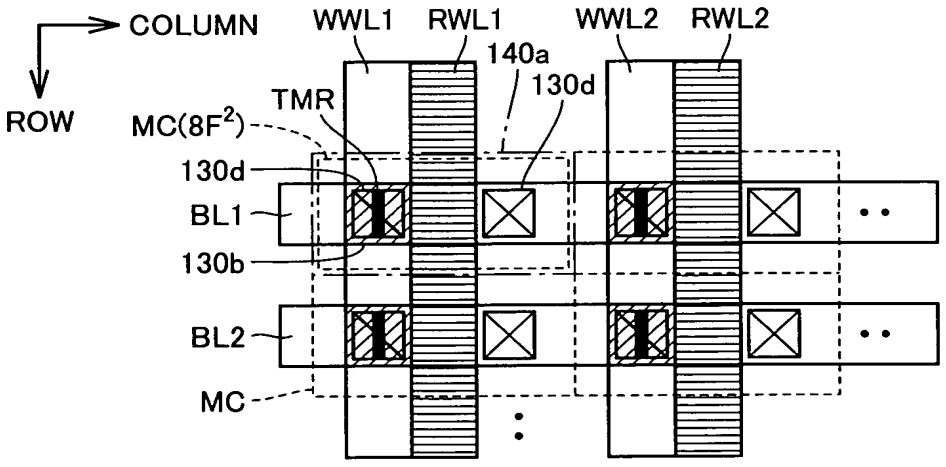
COLUMN
ROW
WWL1
RWL1
WWL2
RWL2
140a
130d
TMR
MC(8F²)
130d
BL1
130b
BL2
MC

FIG.20

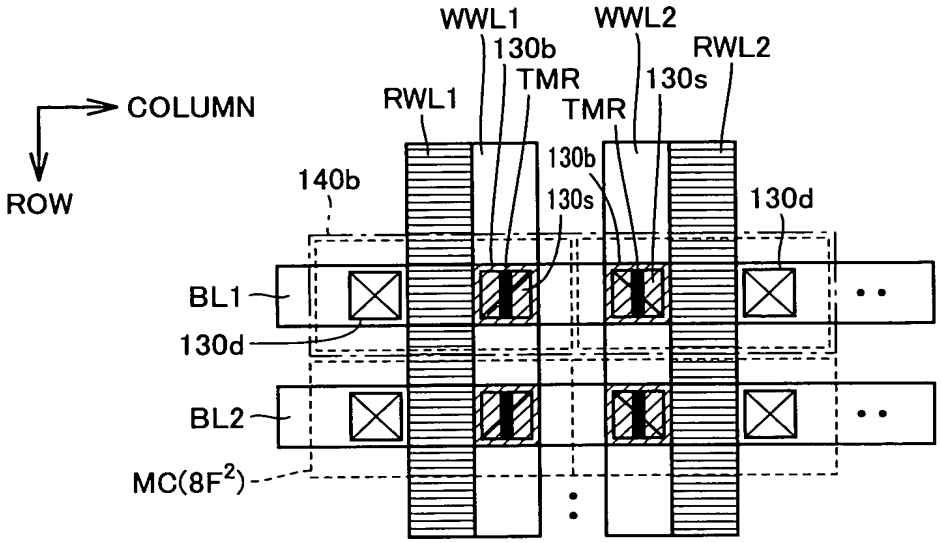
WWL1
WWL2
130b
RWL2
TMR
130s
RWL1
TMR
COLUMN
ROW
130b
140b
130s
130d
BL1
130d
BL2
MC(8F2)

FIG.21

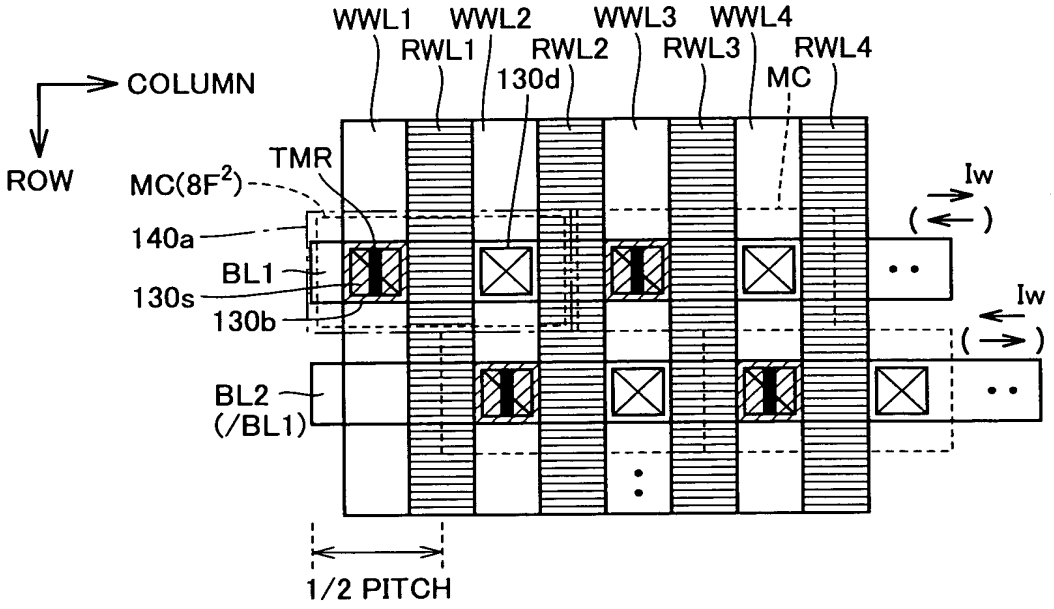
WWL1
WWL2
WWL3
WWL4
RWL1
RWL2
RWL3
RWL4
130d
MC
COLUMN
ROW
TMR
MC(8F2)
Iw
140a
BL1
130s
130b
Iw
BL2
(/BL1)
1/2 PITCH

FIG.22

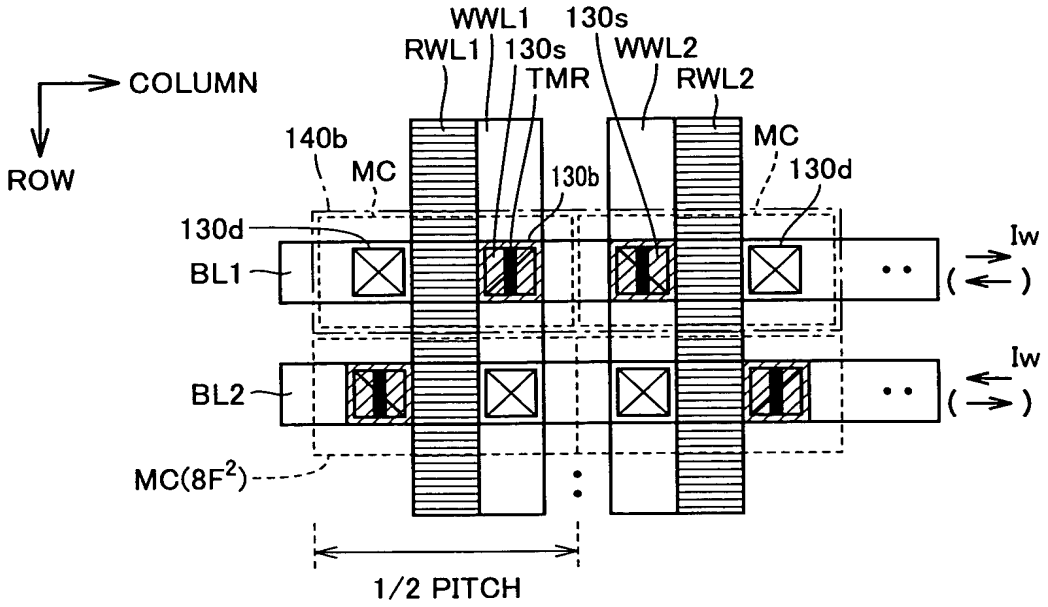

FIG.23

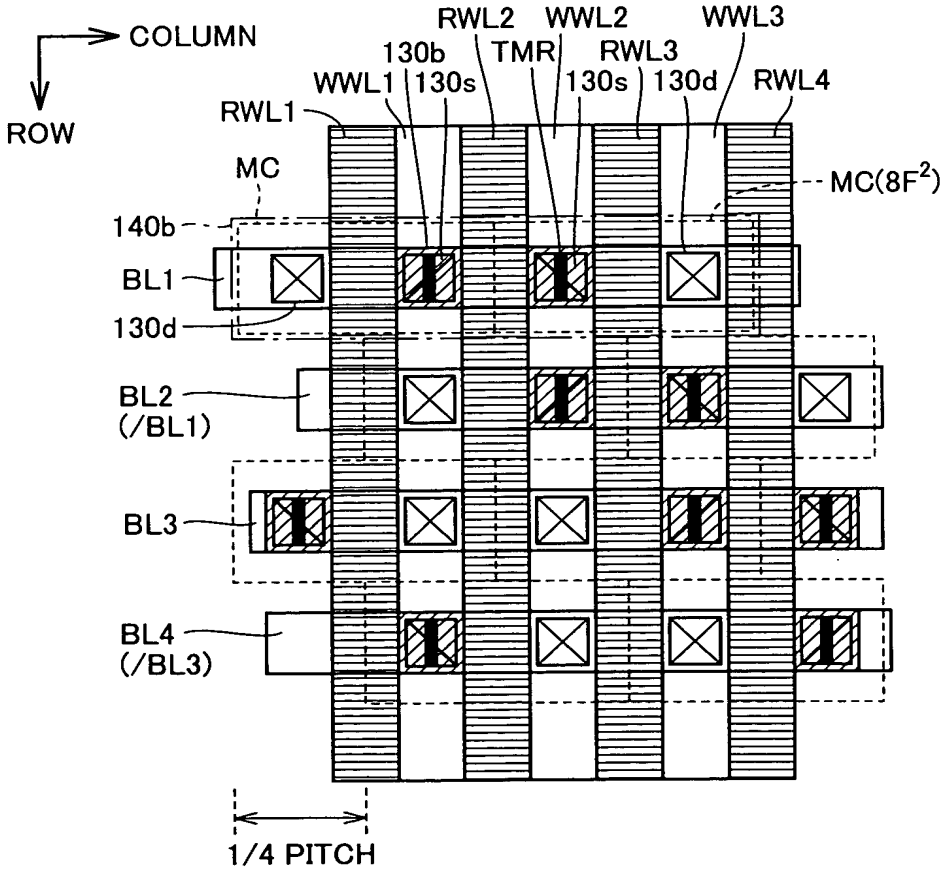

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FIG.24

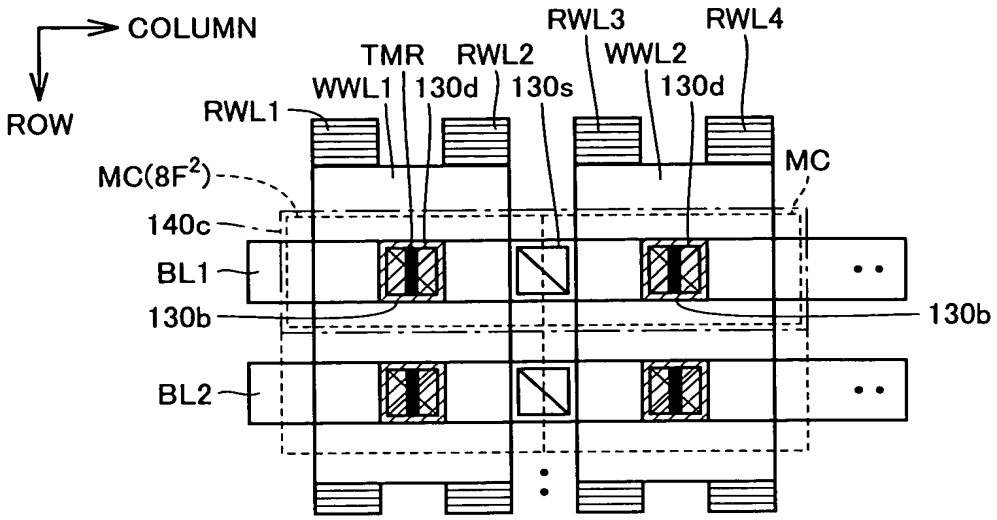
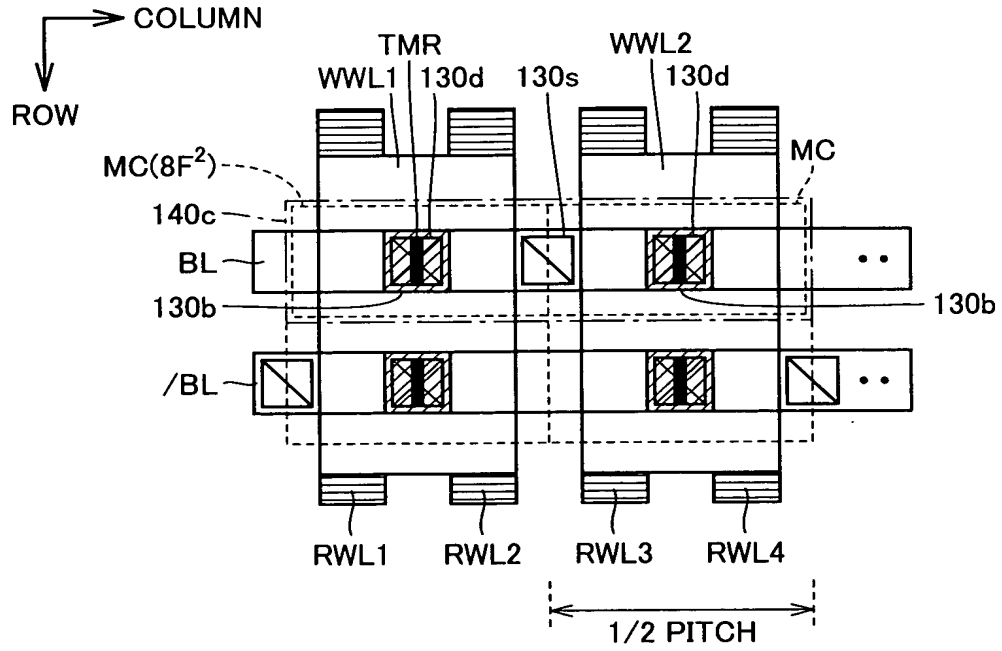


FIG.25



2005084010.04180

FIG.26

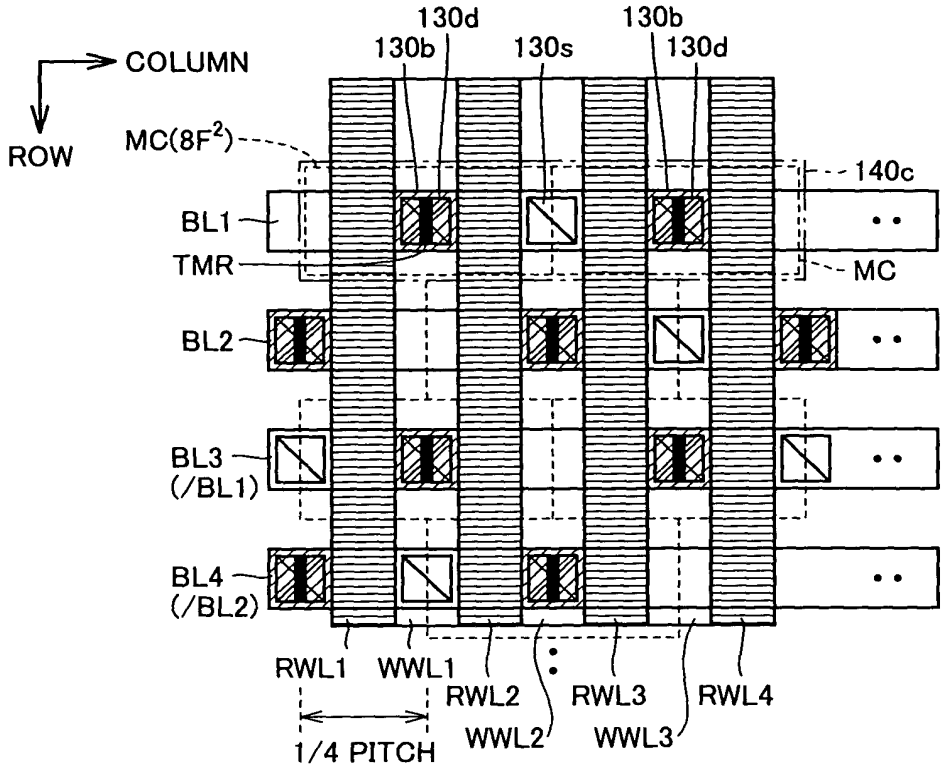

COLUMN
ROW
MC(8F²)
130d
130b
130s
130b
130d
140c
BL1
TMR
MC
BL2
BL3
(/BL1)
BL4
(/BL2)
RWL1
WWL1
RWL2
RWL3
RWL4
WWL2
WWL3
1/4 PITCH

FIG.27

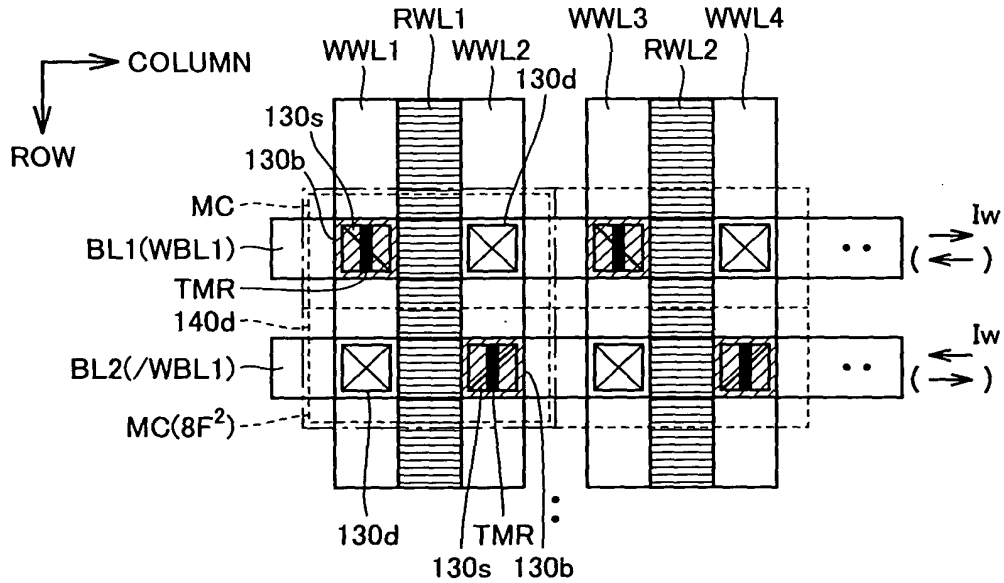

COLUMN
ROW
RWL1
WWL1
WWL2
130d
WWL3
WWL4
RWL2
130s
130b
MC
BL1(WBL1)
TMR
140d
BL2(/WBL1)
MC(8F²)
Iw
Iw
130d
TMR
130s
130b

FIG.28

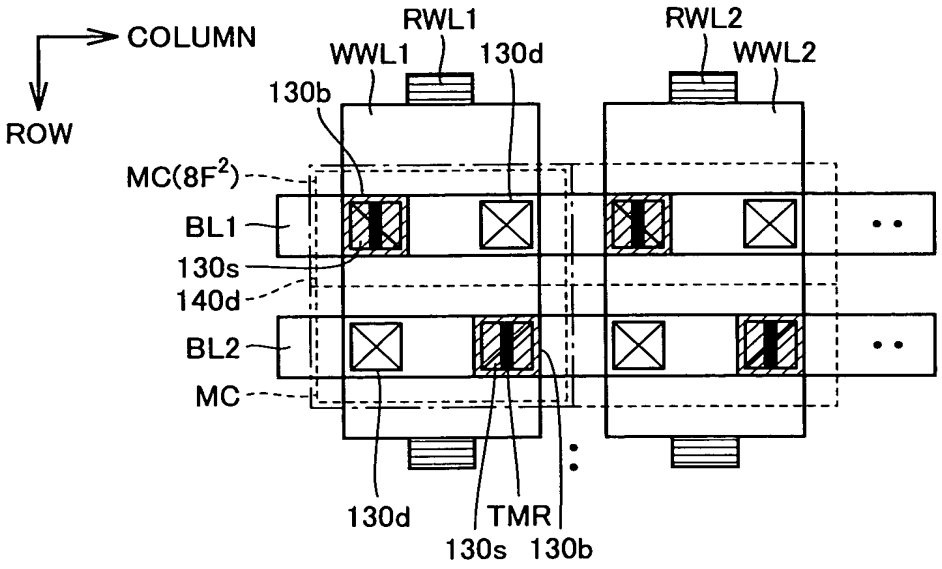

COLUMN
ROW
RWL1
WWL1
130d
RWL2
WWL2
130b
MC(8F2)
BL1
130s
140d
BL2
MC
130d
TMR
130s
130b

FIG.29

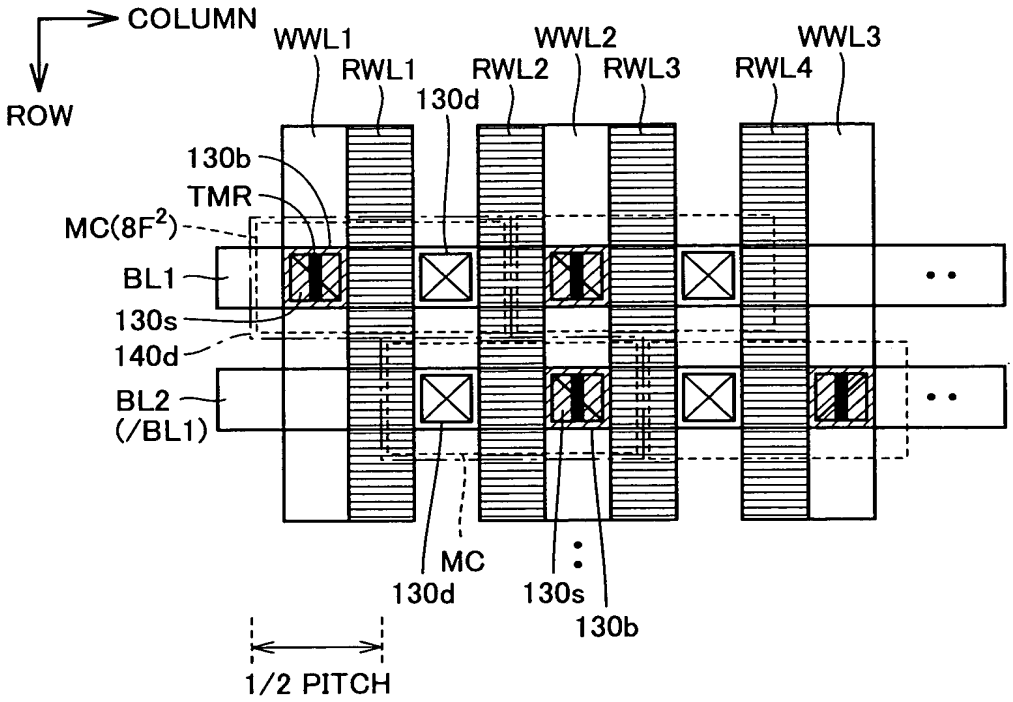

COLUMN
ROW
WWL1
RWL1
130d
WWL2
RWL2
RWL3
WWL3
RWL4
130b
TMR
MC(8F2)
BL1
130s
140d
BL2
(/BL1)
MC
130d
130s
130b
1/2 PITCH

FIG.30

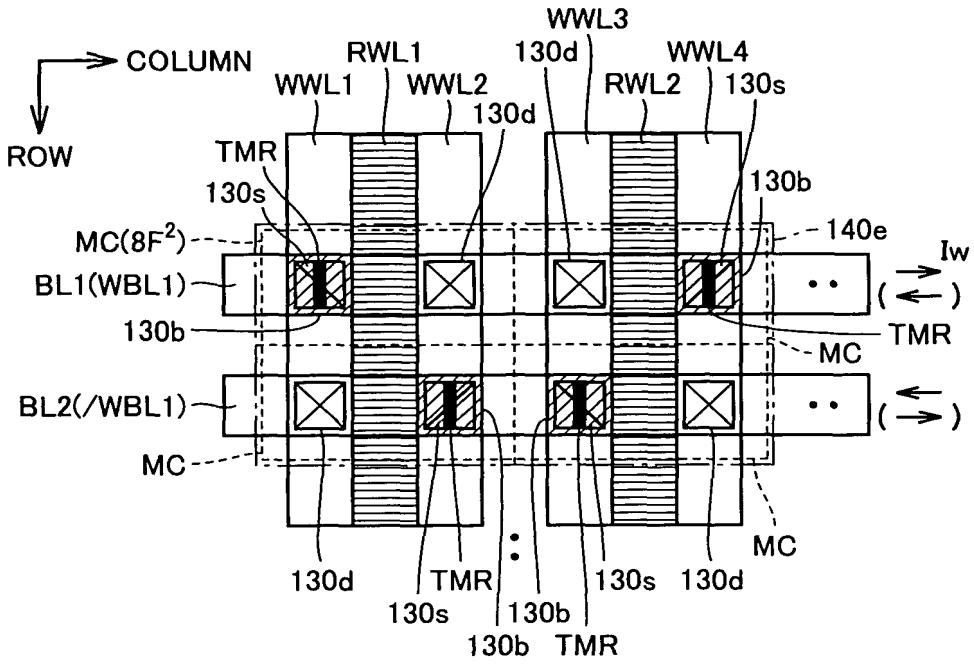

COLUMN
ROW
WWL3
RWL1
130d
WWL4
WWL1
WWL2
RWL2
130s
130d
TMR
130b
130s
140e
MC(8F2)
Iw
BL1(WBL1)
130b
TMR
MC
BL2(/WBL1)
MC
MC
130d
TMR
130s
130b
130s
130d
130b
TMR

FIG.31

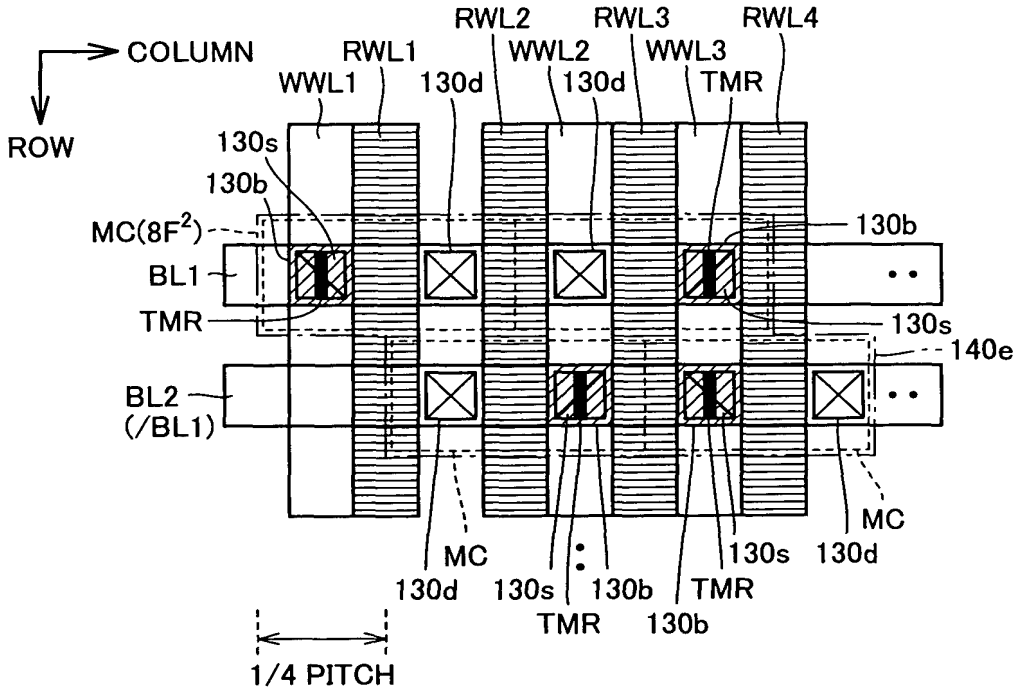

COLUMN
ROW
RWL2
RWL3
RWL4
RWL1
WWL2
WWL3
WWL1
130d
130d
TMR
130s
130b
130b
MC(8F2)
BL1
TMR
130s
140e
BL2
(/BL1)
MC
MC
130d
130s
130b
TMR
130s
130d
TMR
130b
1/4 PITCH

FIG.32

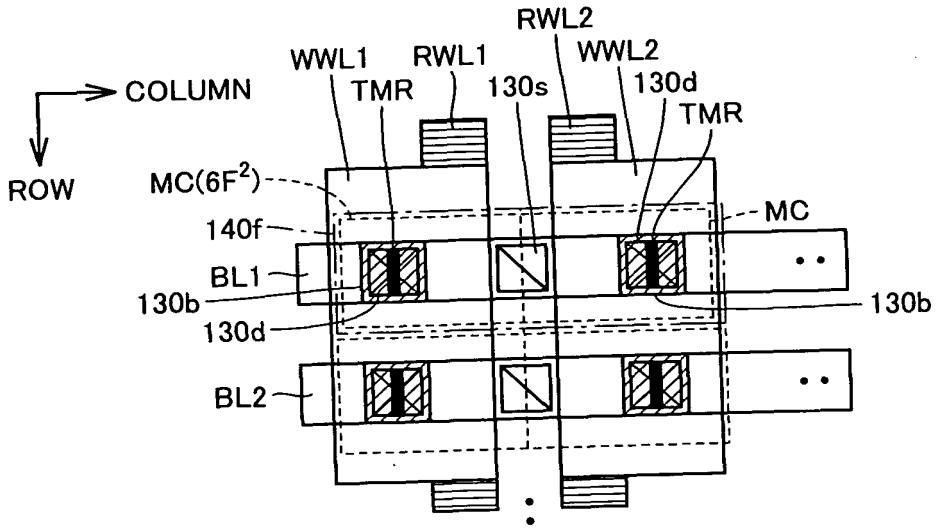

COLUMN
ROW
WWL1
TMR
RWL1
RWL2
WWL2
130s
130d
TMR
MC(6F2)
MC
140f
BL1
130b
130d
130b
BL2

FIG.33

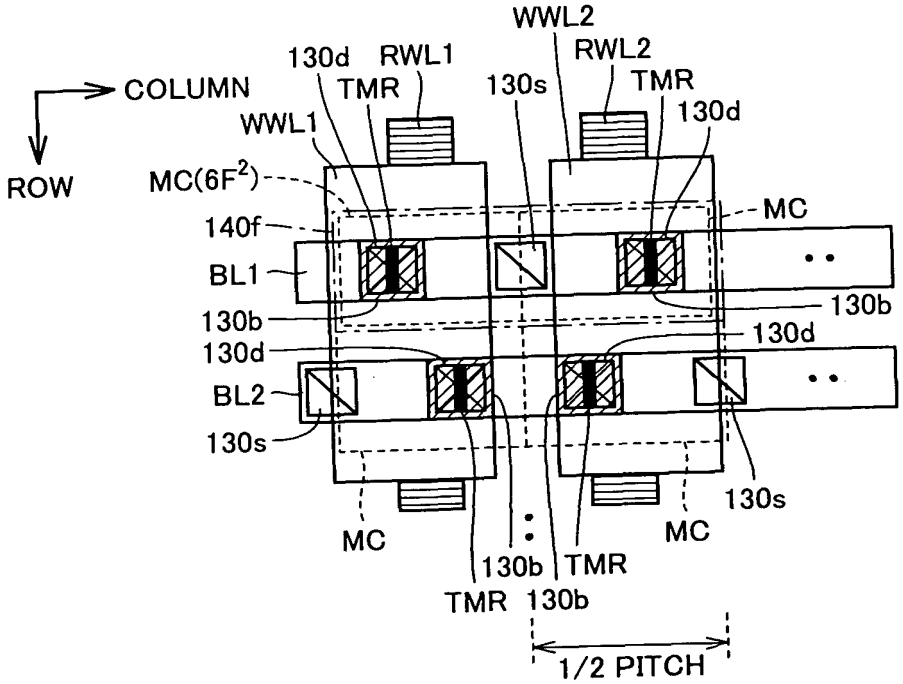

COLUMN
ROW
130d
TMR
RWL1
WWL2
RWL2
130s
TMR
130d
WWL1
MC(6F2)
MC
140f
BL1
130b
130b
130d
130d
BL2
130s
130s
MC
MC
130b
TMR
TMR
130b
1/2 PITCH

FIG.34

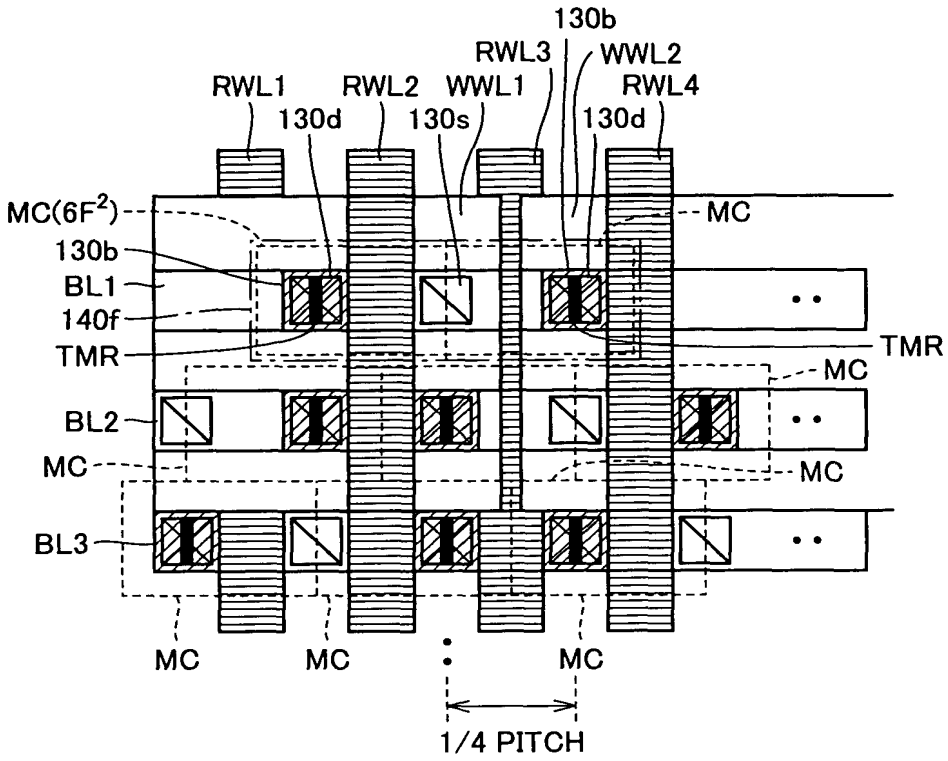

130b
RWL3
WWL2
RWL1
RWL2
WWL1
RWL4
130d
130s
130d
MC(6F2)
MC
130b
BL1
140f
TMR
TMR
MC
BL2
MC
MC
BL3
MC
MC
MC
1/4 PITCH

FIG.35

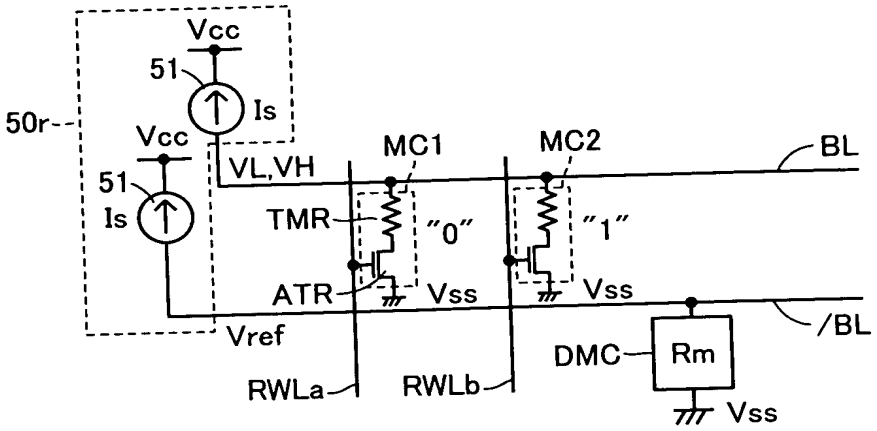


FIG.36

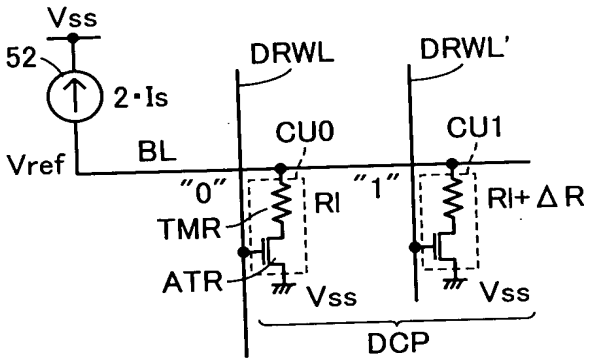


FIG.37

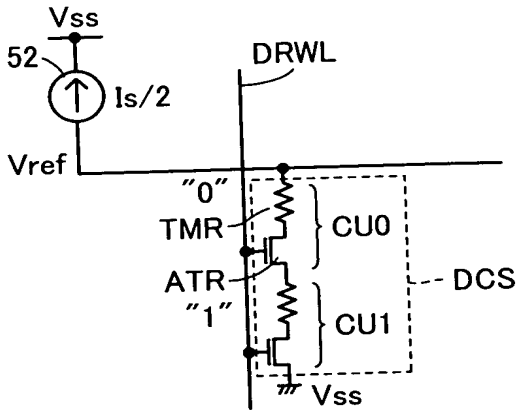


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FIG.38

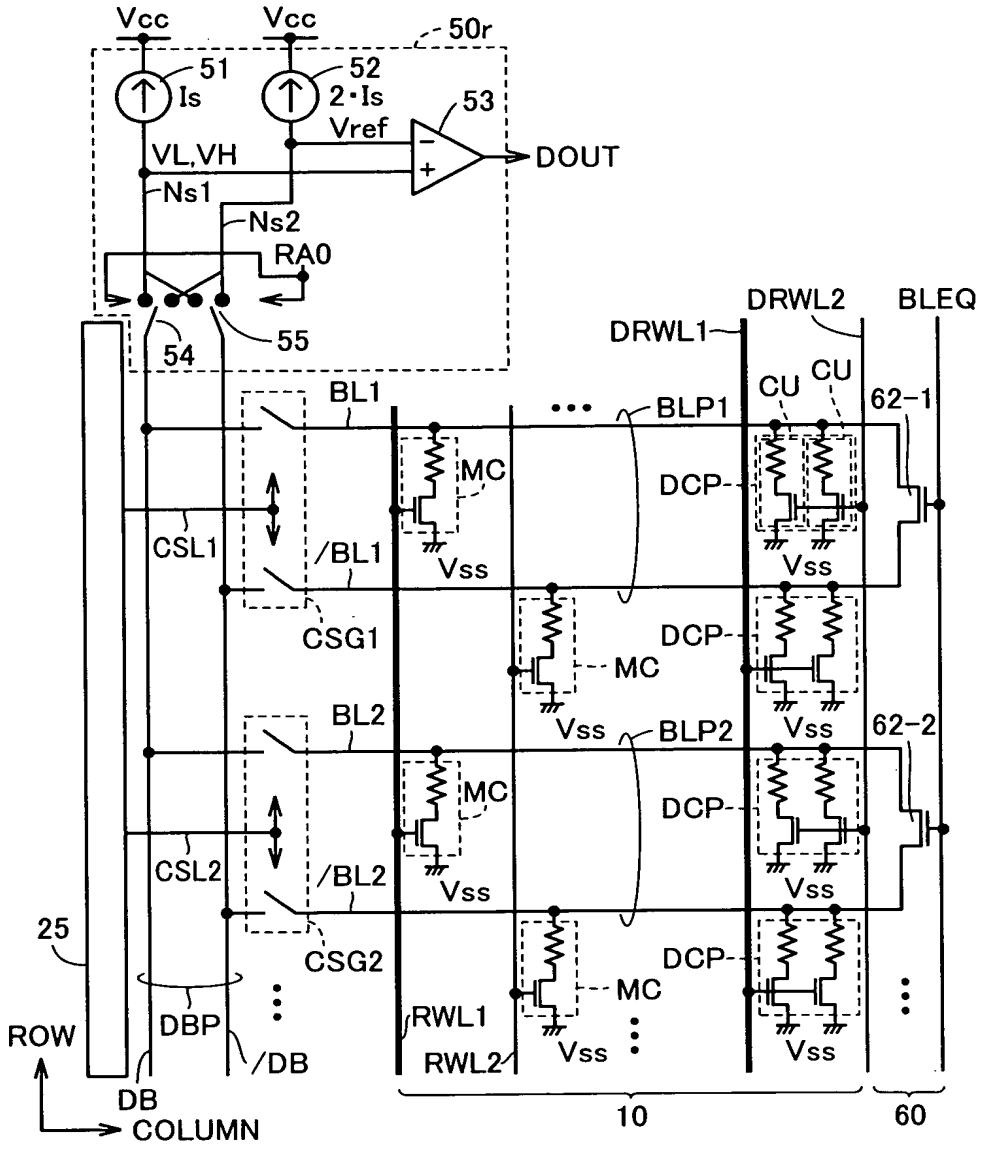
Vcc
Vcc
50r
51
Is
52
2·Is
53
Vref
VL,VH
DOUT
Ns1
Ns2
RA0
54
55
DRWL1
DRWL2
BLEQ
BL1
BLP1
CU
CU
62-1
MC
DCP-
CSL1
/BL1
Vss
CSG1
BL2
BLP2
62-2
CSL2
/BL2
CSG2
25
ROW
DBP
/DB
DB
COLUMN
RWL1
RWL2
10
60

FIG.39

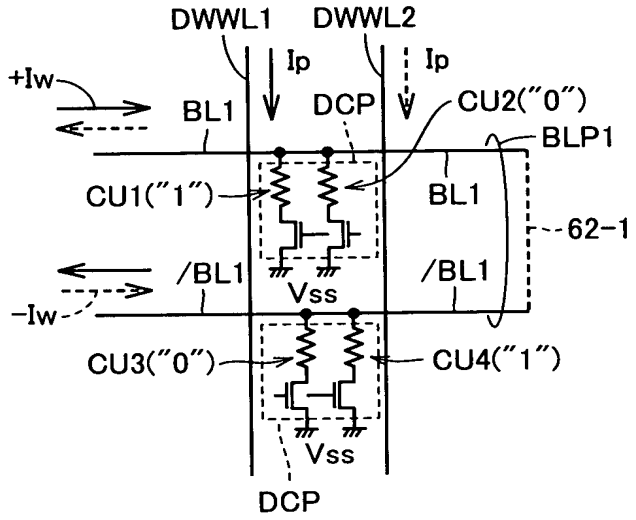

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FIG.40

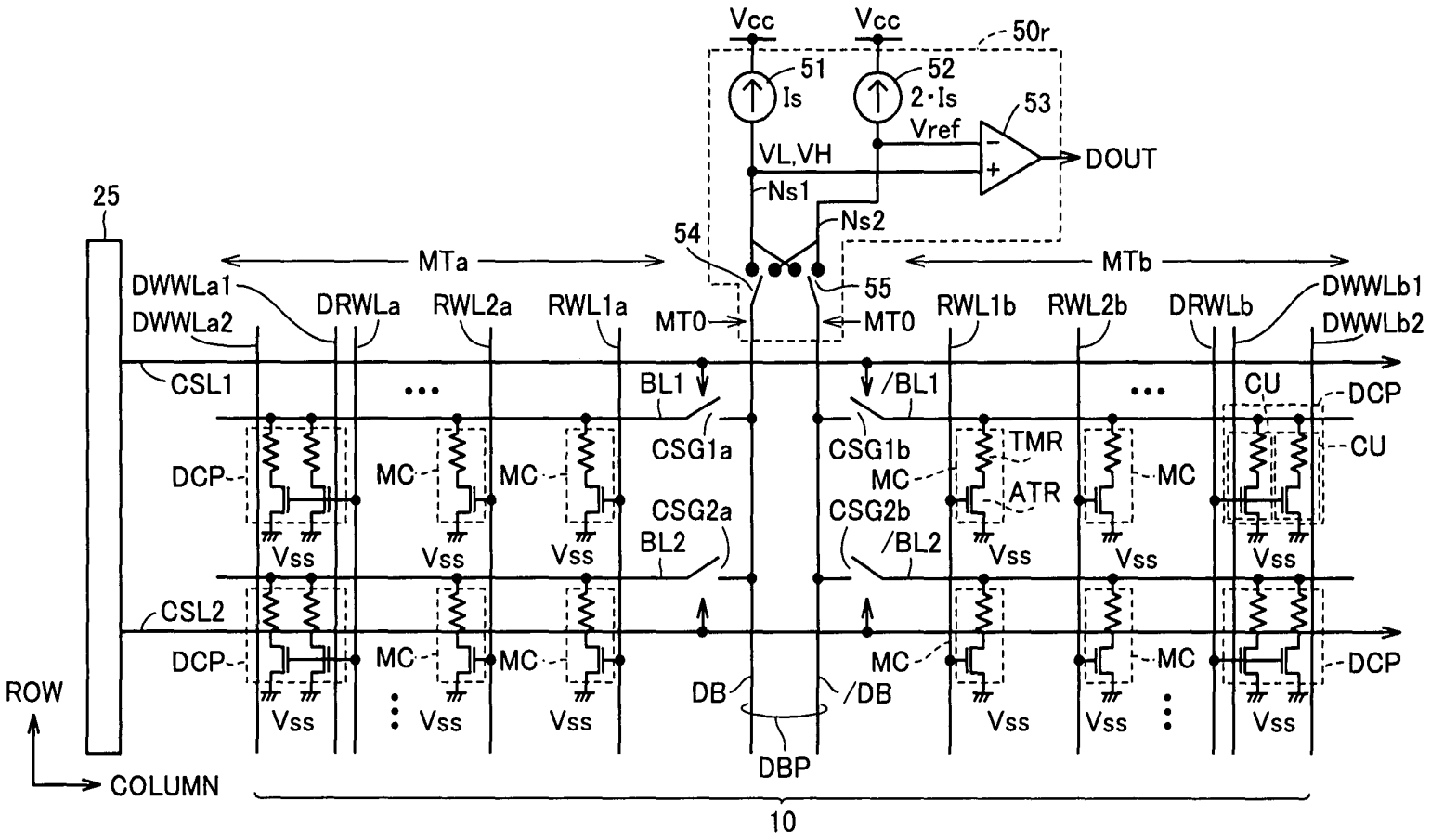

FIG.41

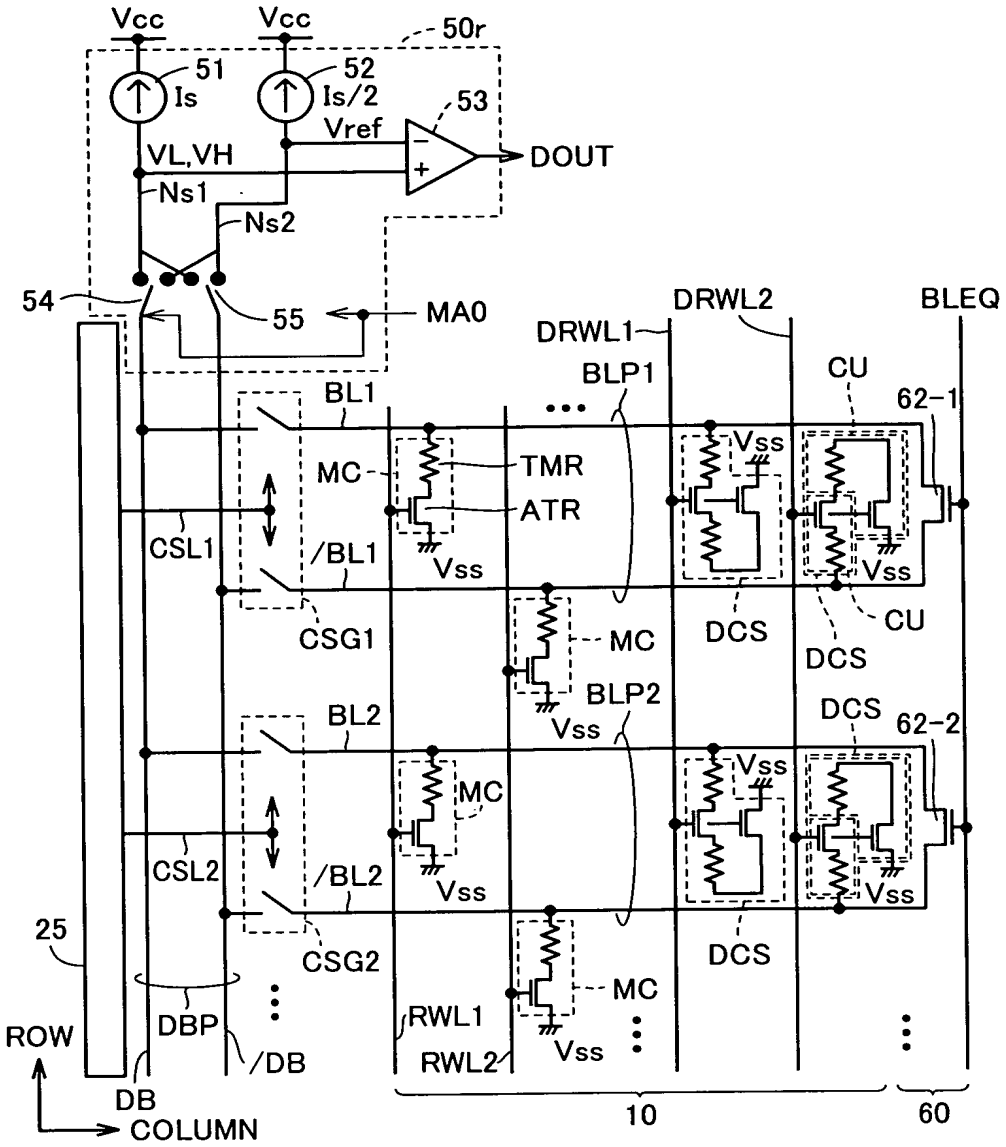

FIG.42

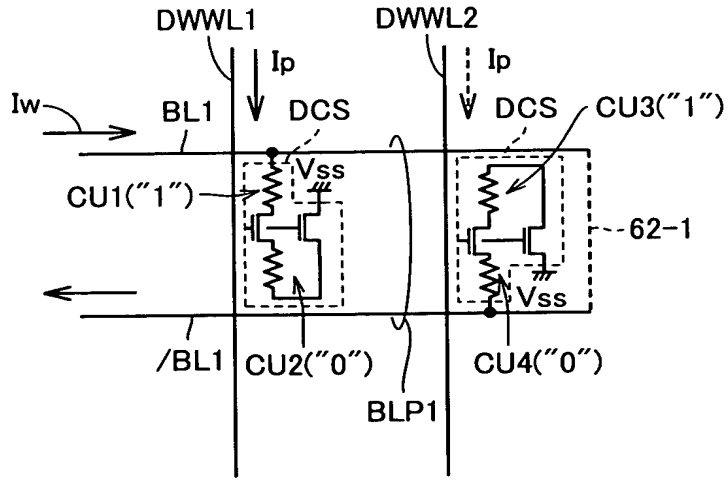

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FIG.43

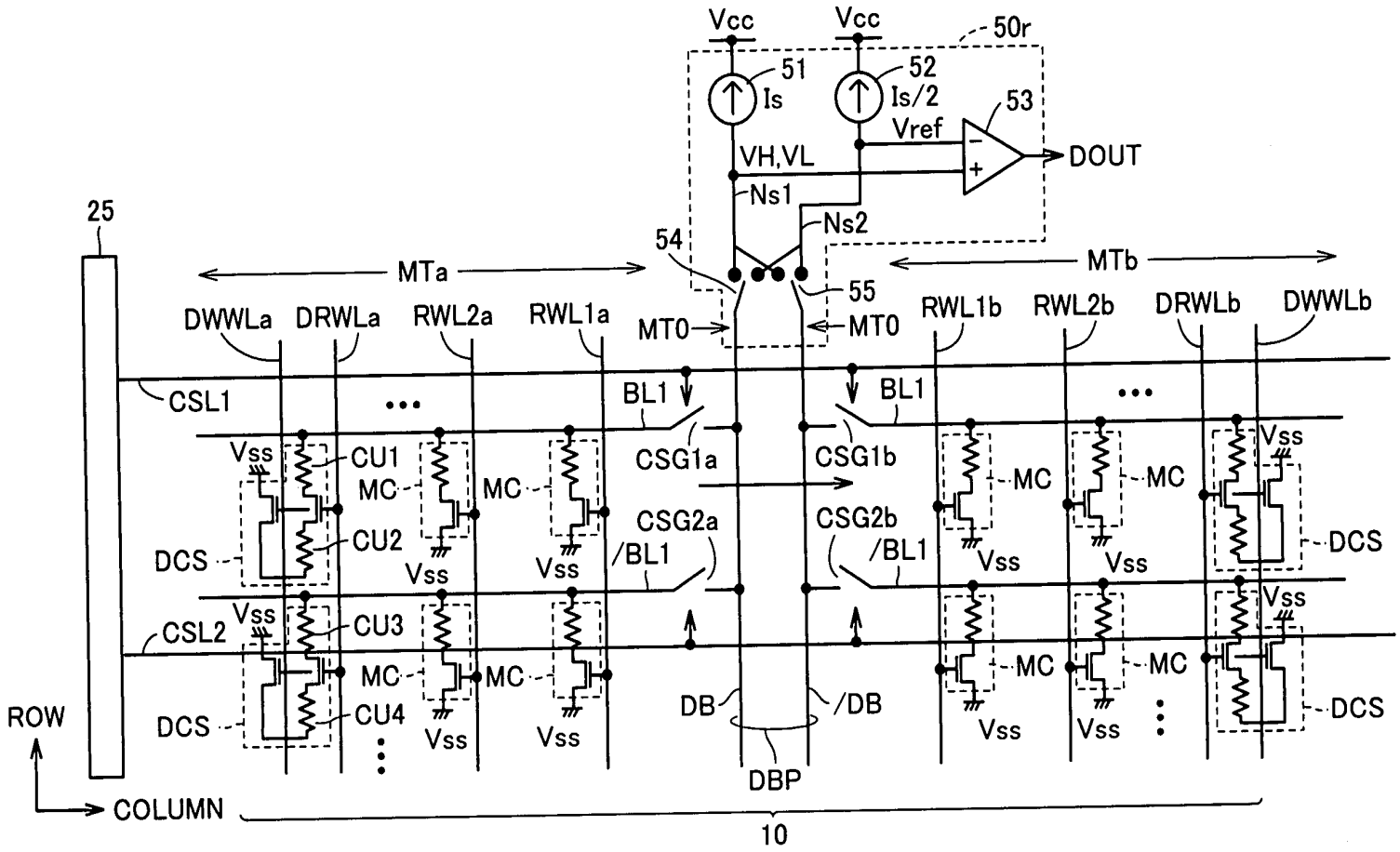


FIG.44

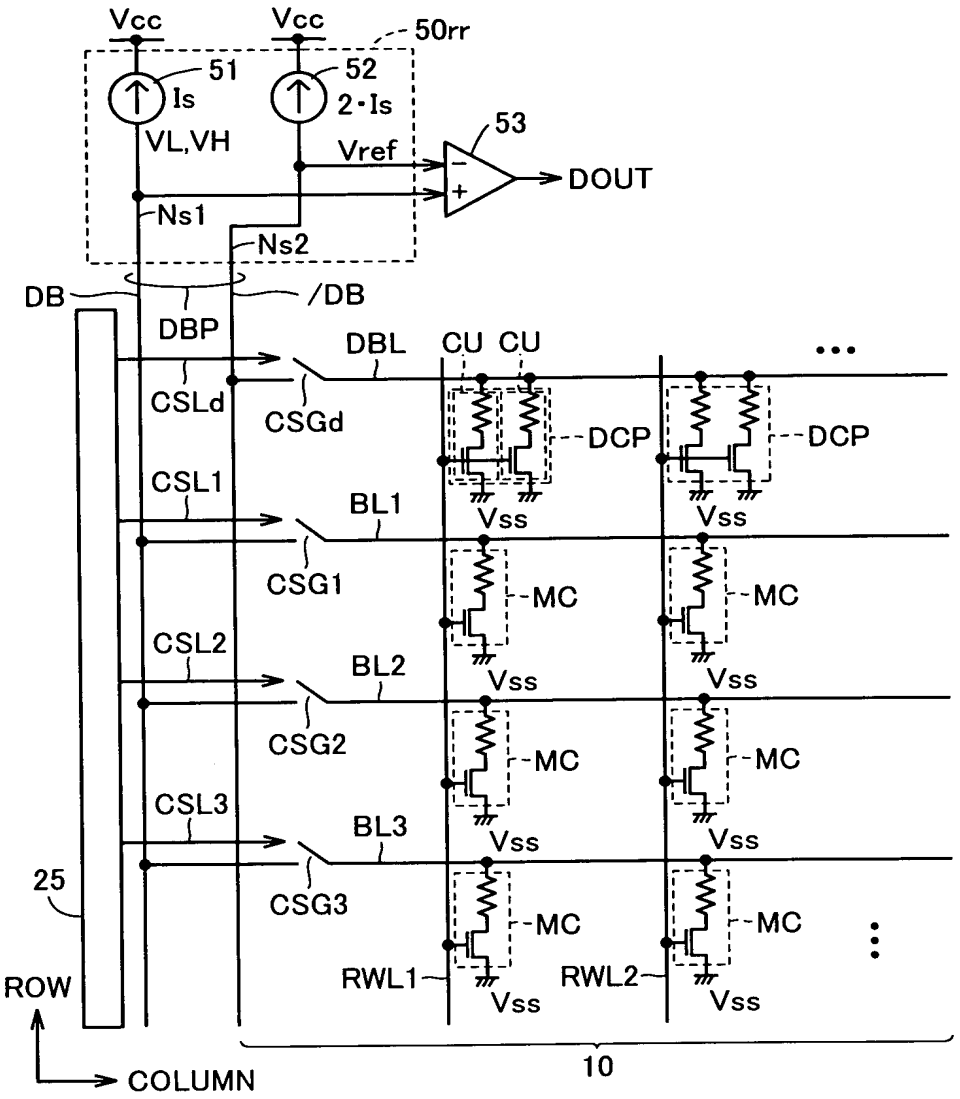

Vcc
Vcc
50rr
51
Is
52
2·Is
VL,VH
Vref
53
DOUT
Ns1
Ns2
DB
/DB
DBP
DBL
CU
CU
CSLd
CSGd
DCP
DCP
CSL1
BL1
Vss
Vss
CSG1
MC
MC
CSL2
BL2
Vss
Vss
CSG2
MC
MC
CSL3
BL3
Vss
Vss
25
CSG3
MC
MC
RWL1
RWL2
Vss
Vss
ROW
COLUMN
10

FIG.45

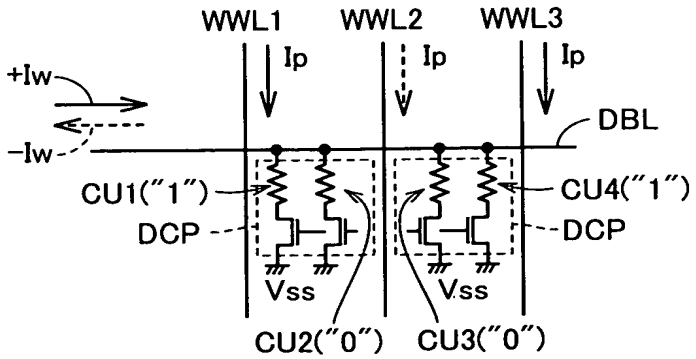

WWL1
WWL2
WWL3
Ip
Ip
Ip
+Iw
-Iw
DBL
CU1("1")
DCP
CU4("1")
DCP
Vss
Vss
CU2("0")
CU3("0")

FIG.46

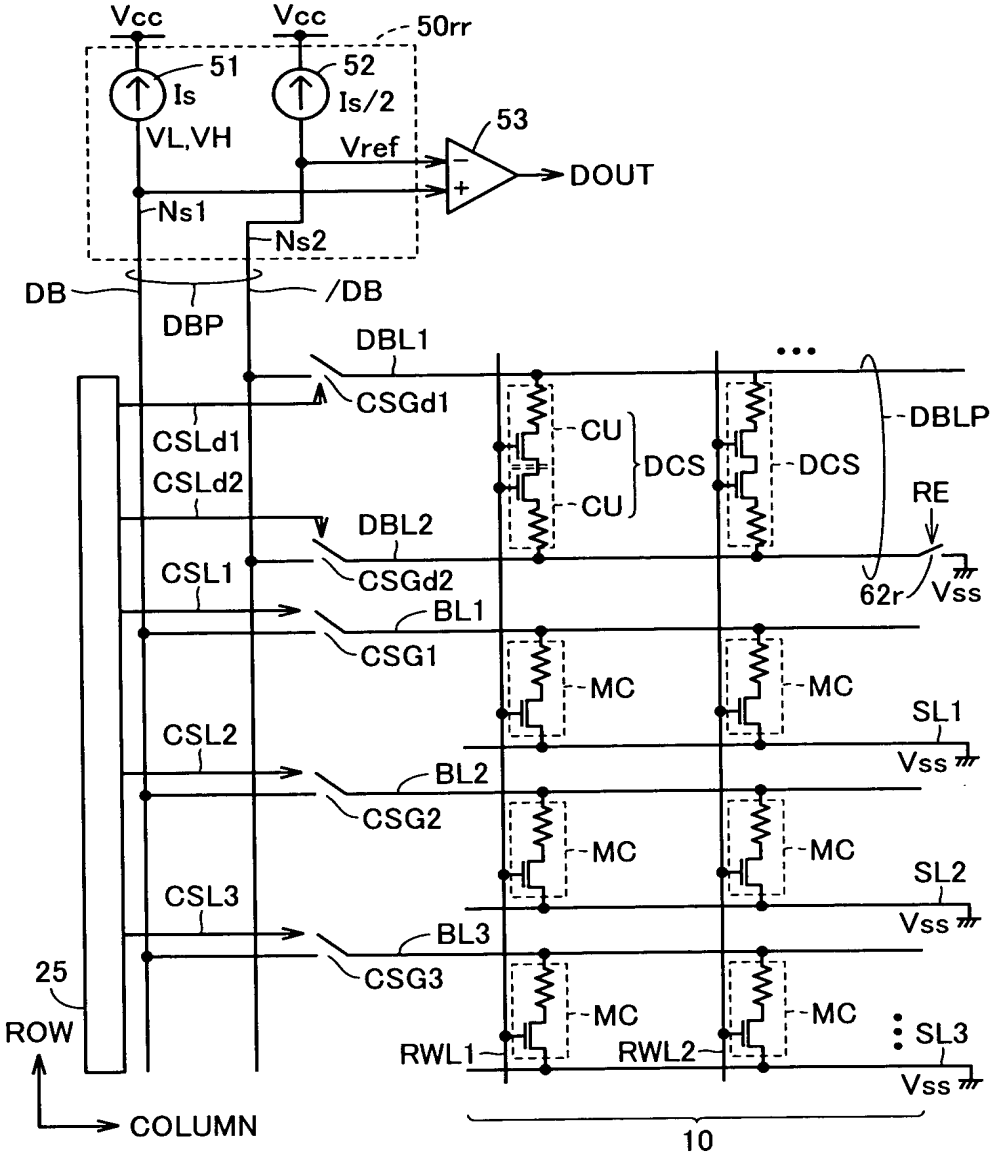

Vcc
Vcc
50rr
51
Is
52
Is/2
VL,VH
Vref
53
DOUT
Ns1
Ns2
DB
/DB
DBP
DBL1
CSGd1
CSLd1
CSLd2
CU
CU
DCS
DCS
DBLP
RE
DBL2
CSGd2
CSL1
62r
Vss
BL1
CSG1
MC
MC
SL1
CSL2
Vss
BL2
CSG2
MC
MC
SL2
CSL3
Vss
BL3
CSG3
25
MC
MC
SL3
ROW
RWL1
RWL2
Vss
COLUMN
10

FIG.47

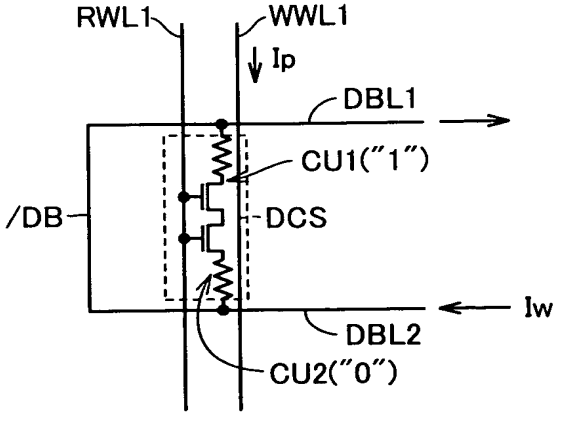

RWL1
WWL1
Ip
DBL1
CU1("1")
/DB
DCS
Iw
DBL2
CU2("0")

FIG.48

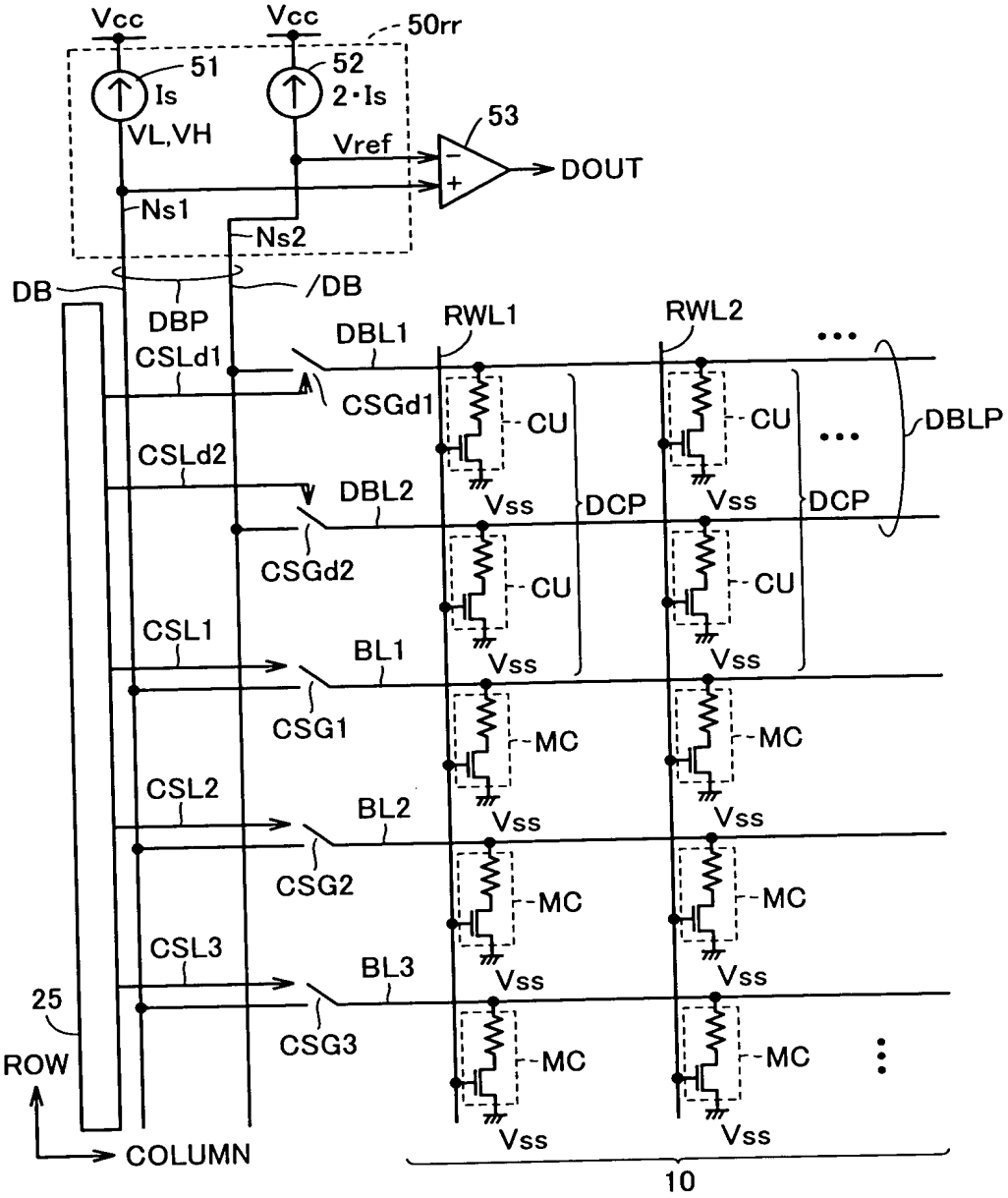
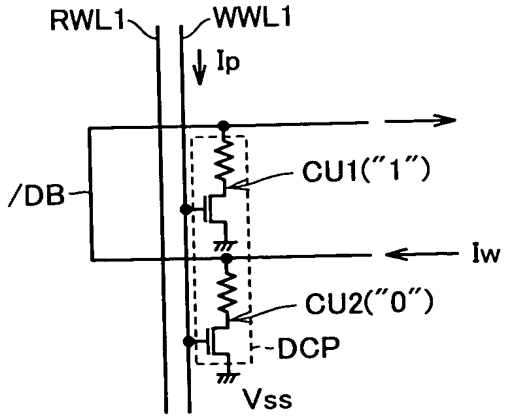


FIG.49



JP2005083100-041802

FIG.50A

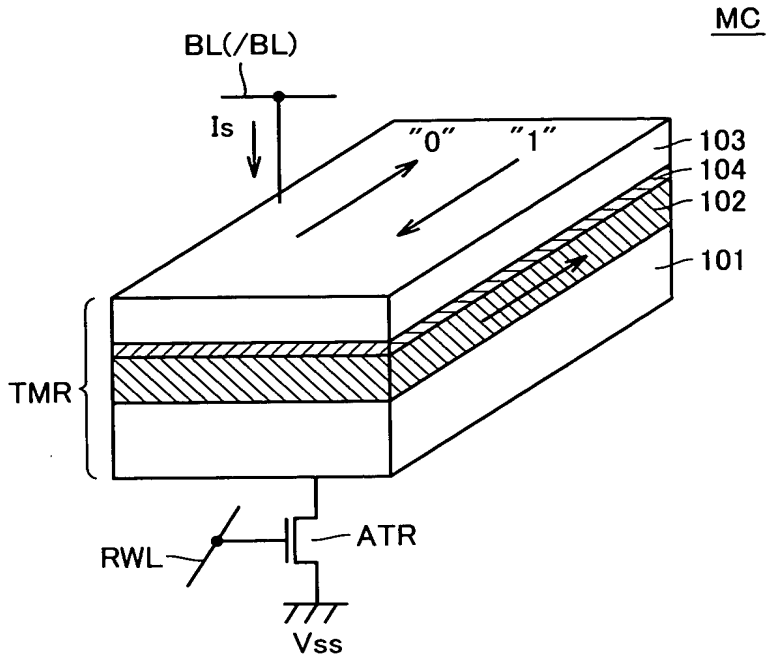
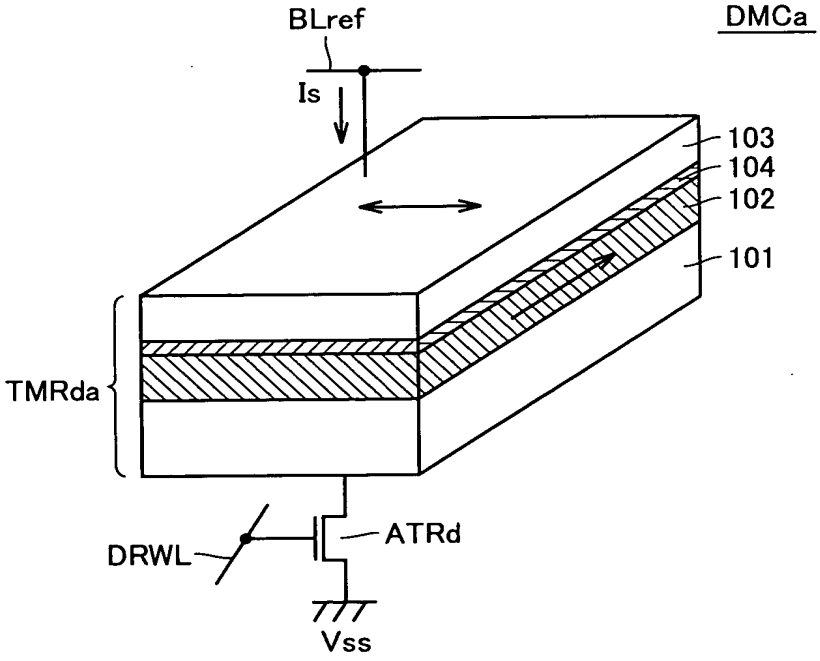


FIG.50B



US2005018502

FIG.51

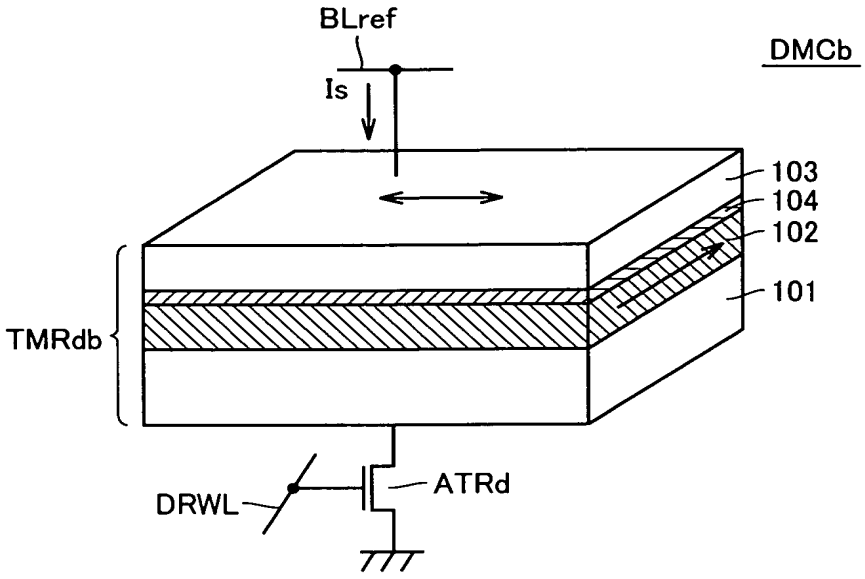


FIG.52

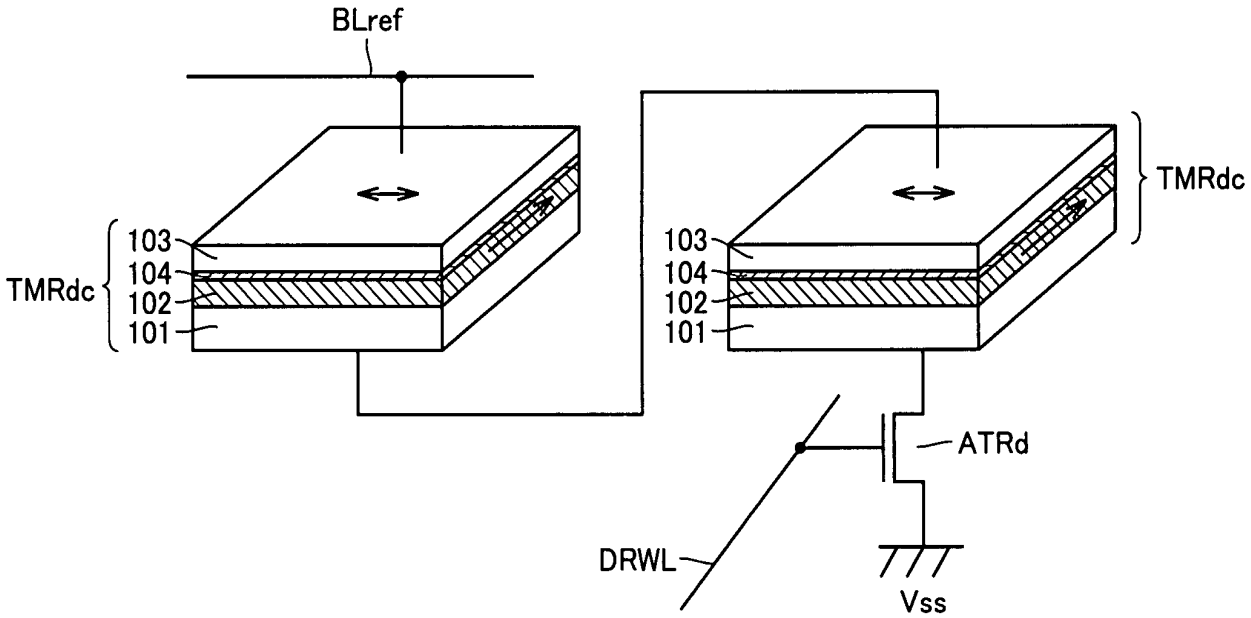

BLref
TMRdc
103
104
102
101
TMRdc
103
104
102
101
TMRdc
ATRd
DRWL
Vss

FIG.53

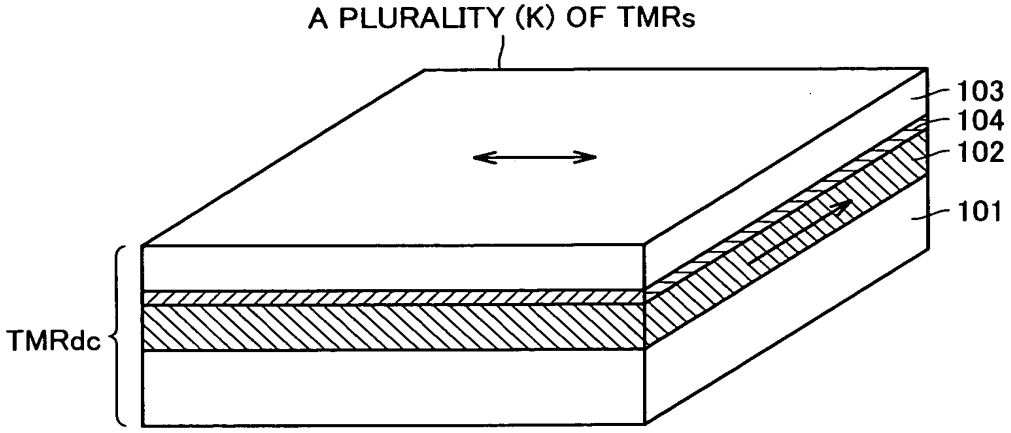

A PLURALITY (K) OF TMRs
103
104
102
101
TMRdc

FIG.54

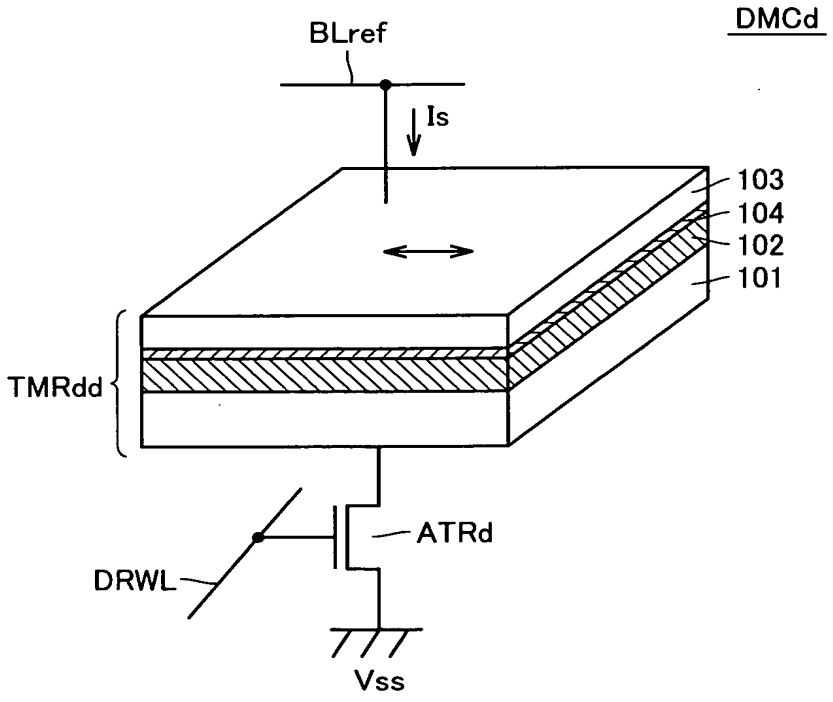

DMCd
BLref
Is
103
104
102
101
TMRdd
ATRd
DRWL
Vss

FIG.55

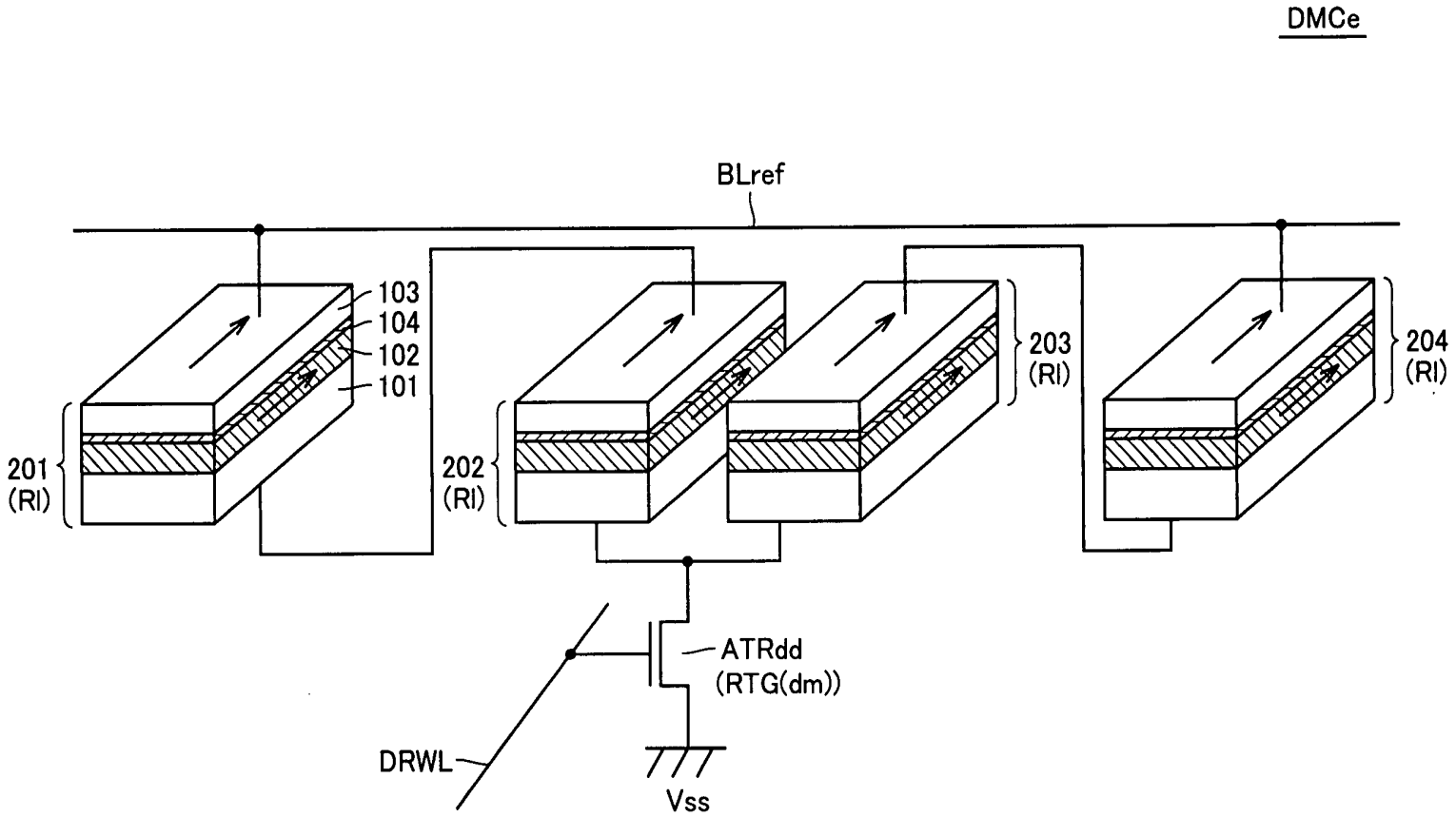

DMCe
BLref
103
104
102
101
201
(RI)
202
(RI)
203
(RI)
204
(RI)
ATRdd
(RTG(dm))
DRWL
Vss

FIG.56

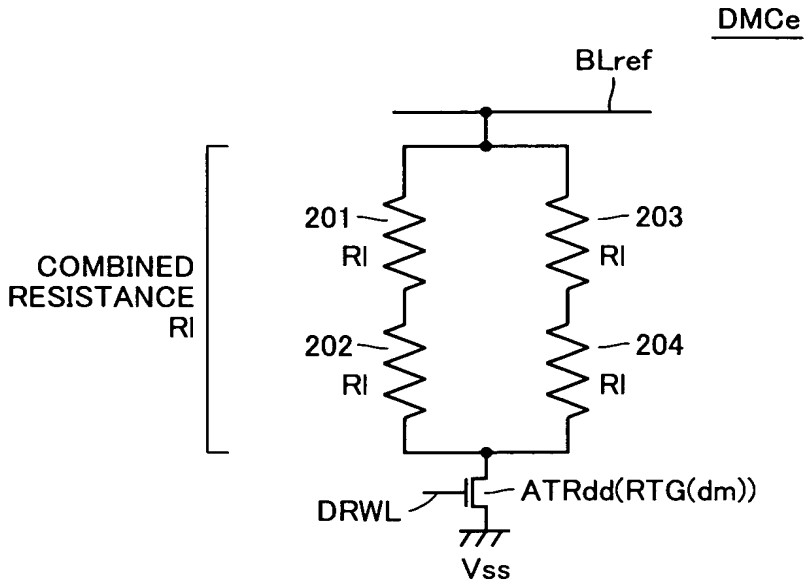
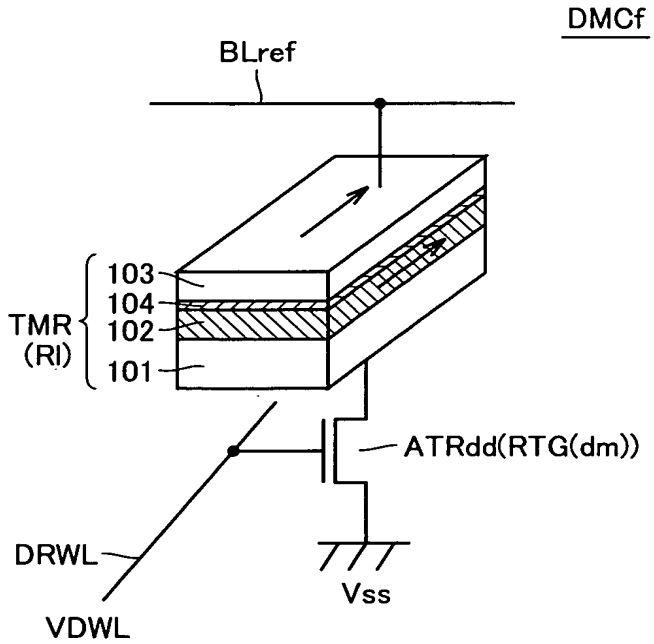


FIG.57



2006-0340-0074 "0340800600"

FIG.58

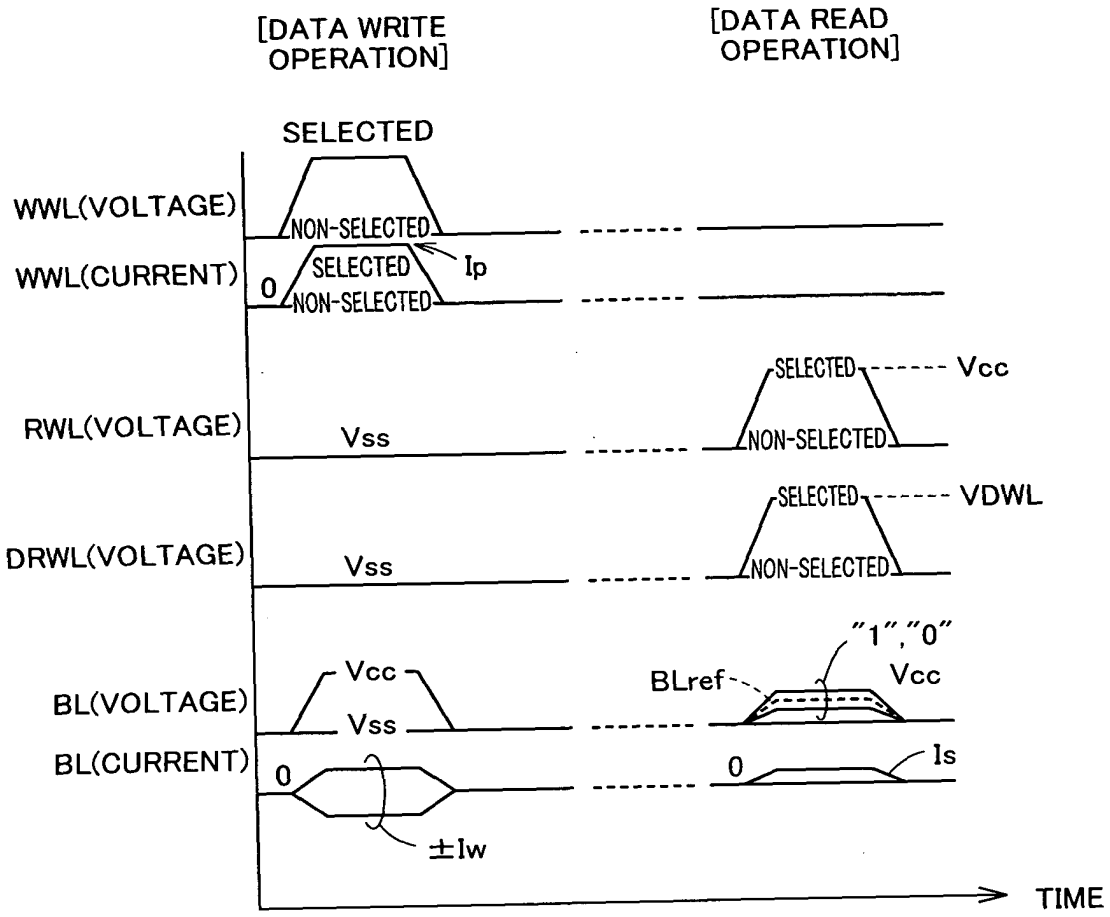

[DATA WRITE OPERATION]
[DATA READ OPERATION]
SELECTED
WWL(VOLTAGE)
NON-SELECTED
WWL(CURRENT)
0
SELECTED
NON-SELECTED
Ip
RWL(VOLTAGE)
Vss
SELECTED
Vcc
NON-SELECTED
DRWL(VOLTAGE)
Vss
SELECTED
VDWL
NON-SELECTED
BL(VOLTAGE)
Vcc
Vss
BLref
"1","0"
Vcc
BL(CURRENT)
0
±Iw
0
Is
TIME

FIG.59

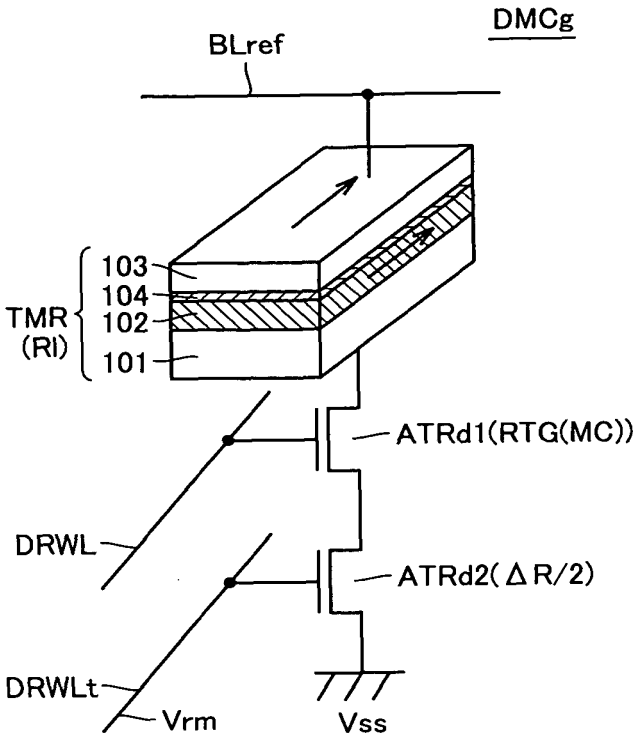

DMCg
BLref
103
104
102
101
TMR
(RI)
ATRd1(RTG(MC))
DRWL
ATRd2(ΔR/2)
DRWLt
Vrm
Vss

FIG.60

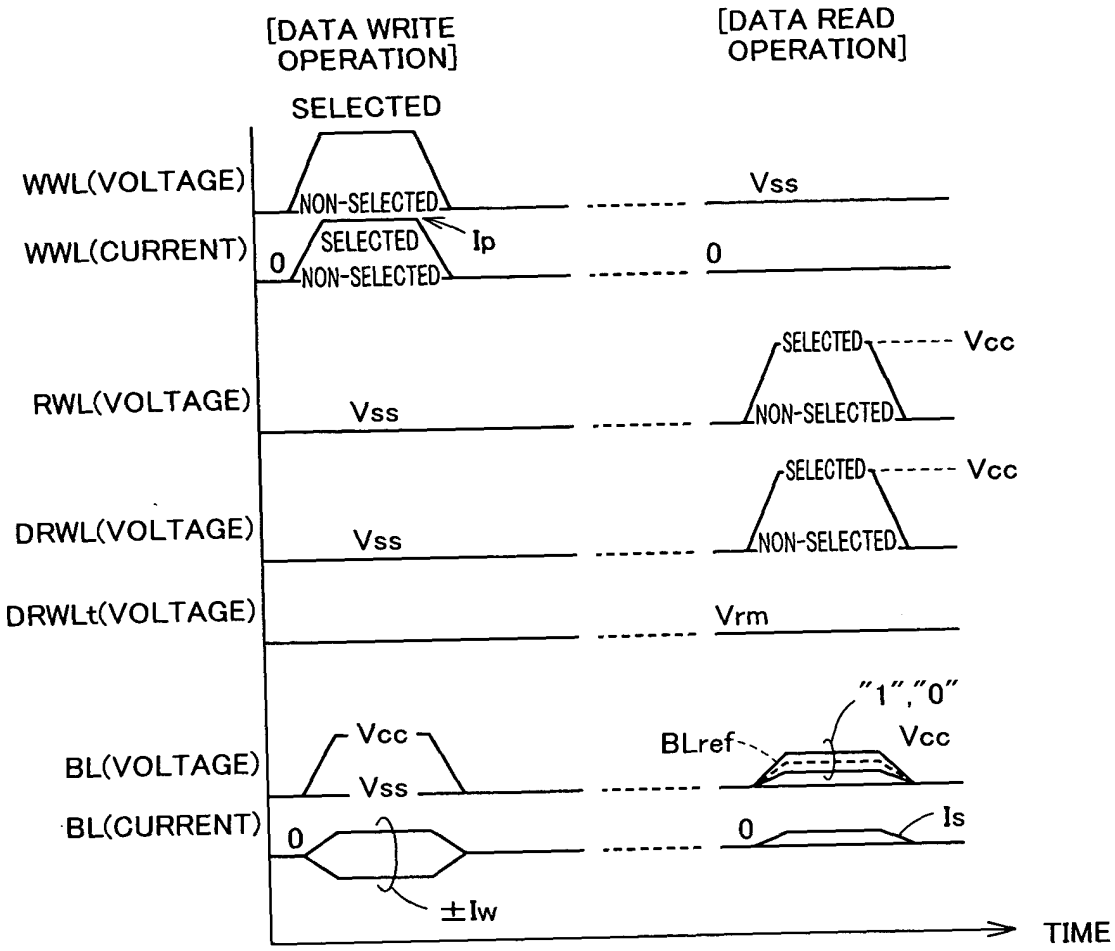

[DATA WRITE OPERATION]
[DATA READ OPERATION]
SELECTED
WWL(VOLTAGE)
NON-SELECTED
Vss
WWL(CURRENT)
0
SELECTED
NON-SELECTED
Ip
0
SELECTED
Vcc
RWL(VOLTAGE)
Vss
NON-SELECTED
SELECTED
Vcc
DRWL(VOLTAGE)
Vss
NON-SELECTED
DRWLt(VOLTAGE)
Vrm
"1","0"
Vcc
BLref
BL(VOLTAGE)
Vcc
Vss
BL(CURRENT)
0
0
Is
±Iw
TIME

FIG.61

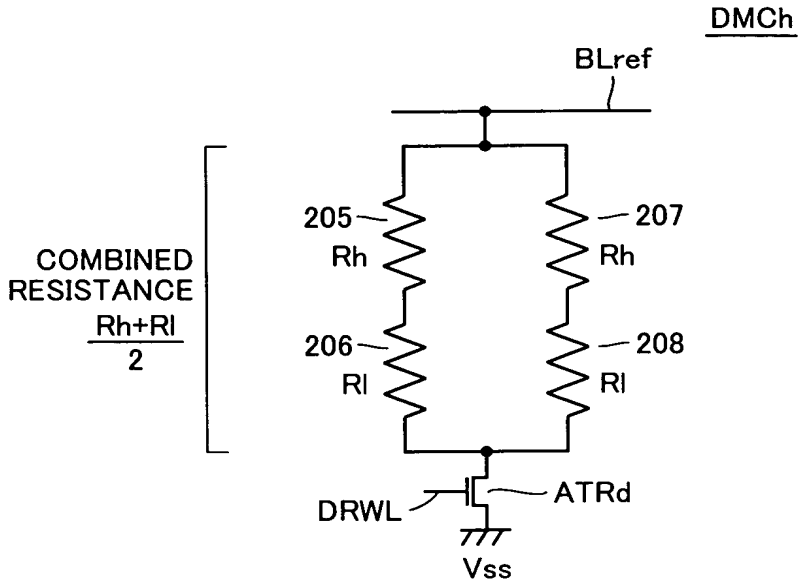


FIG.62

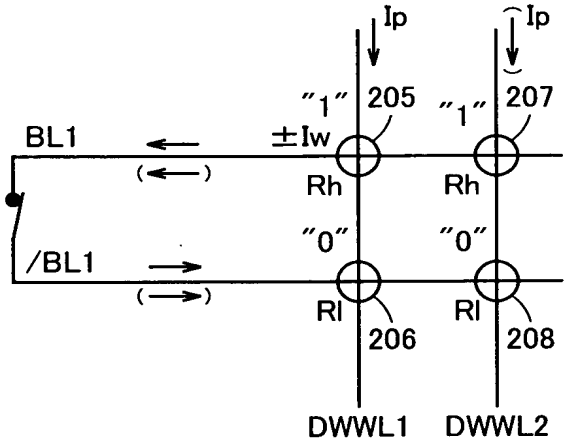


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FIG.63

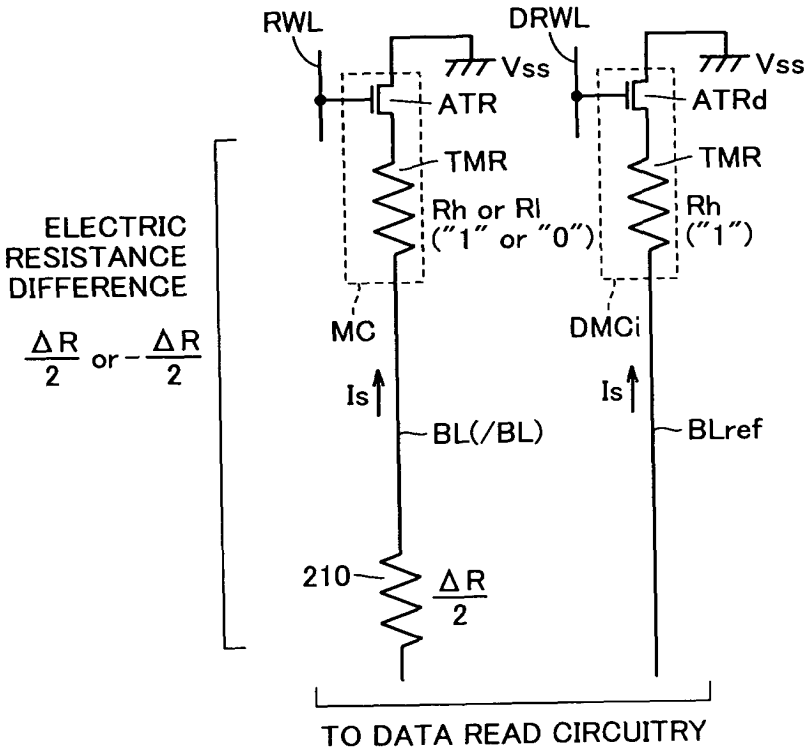
RWL
DRWL
Vss
Vss
ATR
ATRd
TMR
TMR
Rh or Rl
("1" or "0")
Rh
("1")
ELECTRIC
RESISTANCE
DIFFERENCE
ΔR/2 or -ΔR/2
MC
DMCi
Is
Is
BL(/BL)
BLref
210
ΔR/2
TO DATA READ CIRCUITRY

FIG.64

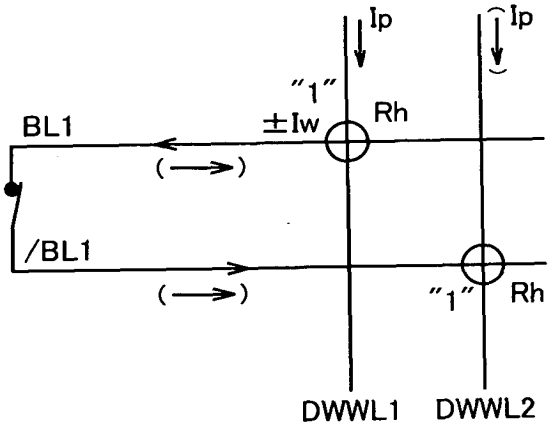
Ip
Ip
"1"
±Iw
Rh
BL1
/BL1
"1"
Rh
DWWL1
DWWL2

FIG.65

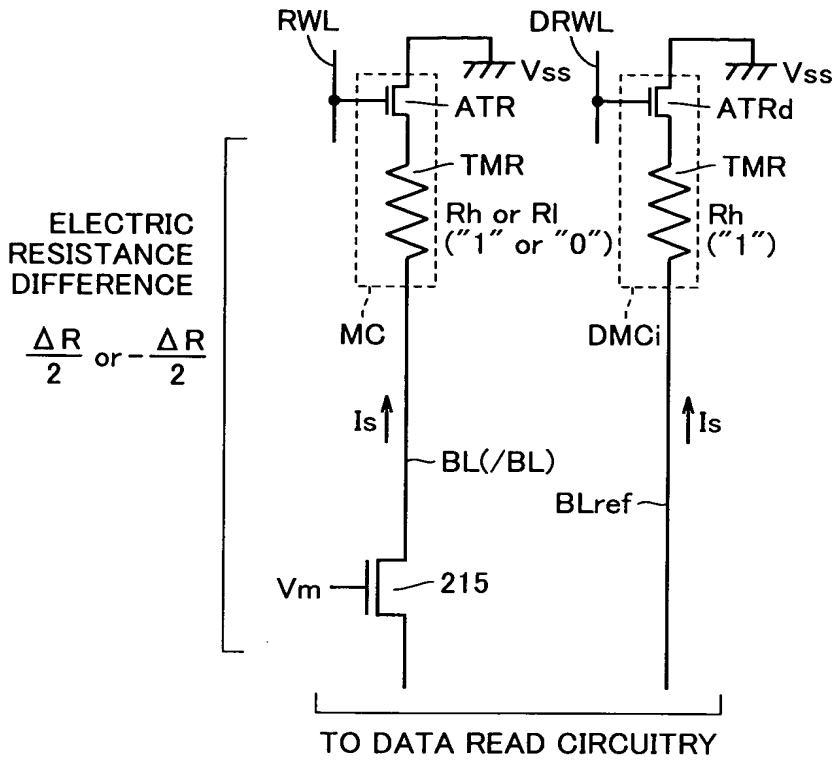

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FIG.66 PRIOR ART

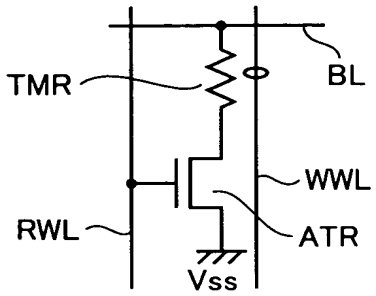

FIG.67 PRIOR ART

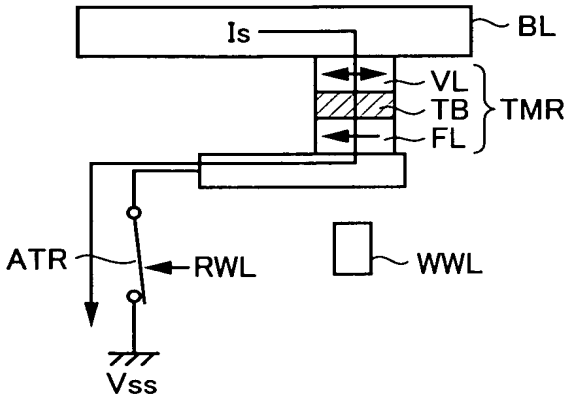

FIG.68 PRIOR ART

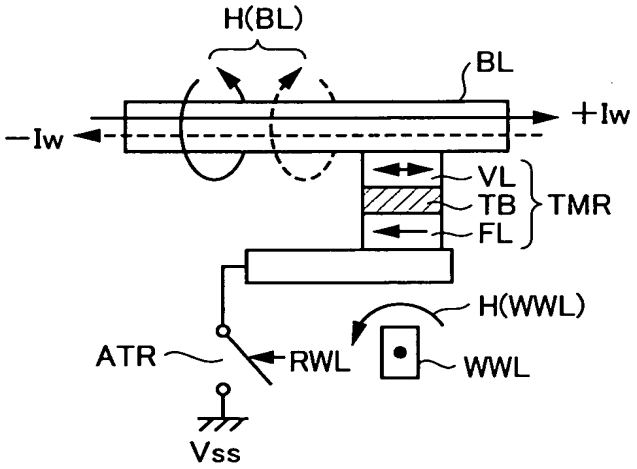
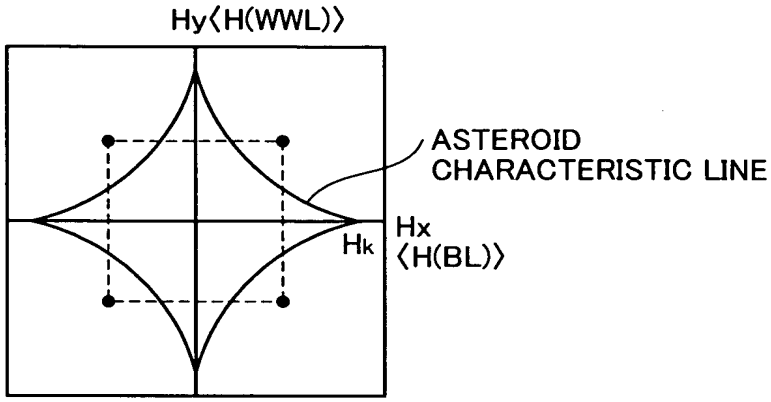
FIG.69 PRIOR ART